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Piezopotential Gated Nanowire–Nanotube Hybrid Field-Effect Transistor

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ABSTRACT We report the first piezoelectric potential gated hybrid field-effect transistors based on nanotubes and nanowires. The device consists of single-walled carbon nanotubes (SWNTs) on the bottom and crossed ZnO piezoelectric fine wire (PFW) on the top with an insulating layer between. Here, SWNTs serve as a carrier transport channel, and a single-crystal ZnO PFW acts as the power-free, contact-free gate or even an energy-harvesting component later on. The piezopotential created by an external force in the ZnO PFW is demonstrated to control the charge transport in the SWNT channel located underneath. The magnitude of the piezopotential in the PFW at a tensile strain of 0.05% is measured to be 0.4–0.6 V. The device is a unique coupling between the piezoelectric property of the ZnO PFW and the semiconductor performance of the SWNT with a full utilization of its mobility. The newly demonstrated device has potential applications as a strain sensor, force/pressure monitor, security trigger, and analog-signal touch screen.

KEYWORDS Piezotronic effect, piezopotential, field-effect transistor, carbon nanotube, ZnO nanowire

Single-walled carbon nanotube (SWNT) field-effect transistor (FET) is one of the most fundamental nanodevices for a range of applications in electronics,[1-5] photonics,[6] and sensors,[7-9] in which the SWNT is connected by two electrodes as the current channel and a third electrode is built on the top/bottom of the SWNT channel as a gate. The carrier transport process in the FET is modulated by an externally applied gate voltage or varying electric field.[10] ZnO is a piezoelectric material that can create an internal piezoelectric potential (piezopotential) in the volume by applying a stress. The existence of the piezopotential not only can drive a transient flow of electrons in the external load to serve as a nanogenerator for energy harvesting[11-14] but also can serve as a gate voltage that tunes/controls the carrier flow through a ZnO nanowire (NW)-based FET,[15-17] in which the gate electrode is absent and the gate voltage is replaced by the piezopotential. Thus, ZnO NWs can give a gate effect to FET nearby only when they are needed; otherwise, it can serve as an energy-harvesting component for the next FET operation. In this paper, we demonstrate the first ZnO NW and SWNT hybrid FET, in which the piezopotential created by an externally applied strain in a ZnO NW serves as a gate voltage for controlling the carrier transport in a SWNT-based current channel located underneath. The ZnO NW serves as an electric-power-free and contact-free gate. This device is a unique coupling between the piezoelectric property of the ZnO NW and the semiconductor performance of the SWNT with a full utilization of its mobility. The newly demonstrated device has potential applications as an energy-harvesting strain sensor, force/pressure monitor, security trigger, and analog-signal touch screen.

An internal field is created in a piezoelectric material once a stress is applied. The tetrahedrally coordinated Zn^{2+} and O^{2-} ions in ZnO have relative displacements once the crystal is subjected to a mechanical stress. The polarization produced by the deformation creates a piezopotential in the crystal (Figure 1A). The magnitude of the piezopotential can be large enough to gate the charge transport process in another nanostructure placed adjacent to ZnO. This is the design here to replace the gate potential for a SWNT FET by the piezopotential to build a FET that is controlled by mechanical deformation. To fabricate such a device, a piezoelectric fine wire (PFW) is laid flat on a FET embedded flexible substrate and fixed at both ends using a polyepoxide; the PFW has no electrical contact with an external source/load (Figure 1B). When the substrate was bent downward, a tensile strain is induced in the ZnO PFW, leading to a piezoelectric potential drop along the wire. Since the diameter of the ZnO wires (~1–3 μm) is much smaller than the thickness of the Kapton substrate (127 μm), the shear strain can be safely neglected.[13] On the basis of a static model calculation,[18] for a ZnO wire with a diameter $d = 4\ \mu$m and length $l = 220\ \mu$m, when a total external force of $f_z = 1\ \mu$N was applied at its one side end, the piezopotential distribution along the bent wire oriented with its c-axis pointing leftward is shown in Figure 1A by ignoring the doping. Under the external deformation, the length of the wire would increase for 0.2 nm, which produces a tensile strain of 1 ×

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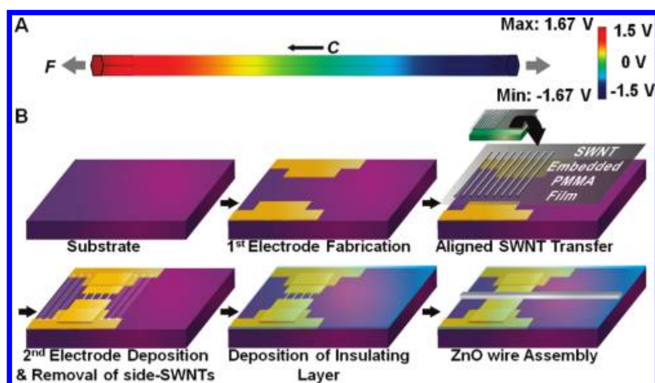

FIGURE 1. Theoretical modeling of piezoelectric potential in a ZnO PFW, and fabrication procedures for the hybrid FET. (A) Plot of piezoelectric potential distribution φ as calculated using a static model without considering doping. The dimension of the wire is width $d = 4\ \mu m$, length $l = 220\ \mu m$. A total external force of $f_z = 1\ \mu N$ was applied at its one end. The piezopotential drop is ~3 V along the *c*-axis of the ZnO PFW. (B) Schematic diagram depicting the process for the wire gated hybrid FET. Both silicon wafer and Kapton film were processed from the beginning to the deposition of insulating layer, but only flexible Kapton substrate was assembled with ZnO PFW as the hybrid FET.

10^{-6}. The piezopotential drop is ~3 V, which is enough to be utilized as a gate bias for controlling current transport in FETs.

Figure 1B is a schematic diagram depicting our device fabrication procedures. We utilized two types of substrates such as $SiO_2/Si(p^{++})$ and Kapton. The first one is only for the quantitative analysis of electronic characteristics of SWNT FETs; the latter is for the piezopotential gated hybrid FETs reported here. Large-sized metal electrodes were fabricated on both substrates as contact pads for electrical measurements. Afterward, SWNTs grown on quartz substrate (see Figure 2A) were transferred to metal patterned substrates using the PMMA transfer method.[19−21] In this case, well-aligned SWNTs were chosen to minimize external strain exertion to them. When an external deformation was applied perpendicular to the direction of the aligned SWNTs, the strain induced in SWNTs could be neglected. Well-aligned SWNTs used here were prepared by a selective growing process for the FET channel, which produces SWNTs with over 95% being semiconducting.[20] To achieve stable source−drain contact between SWNTs and metal pads, an additional photolithography process was implemented following a conventional metal lift-off process to form fully contacted electrodes, resulting in a 2 μm gap SWNT channel. Ultrasonication or taping detachment was applied to remove the nonfully two-end-contacted SWNTs. After attaching the SWNT FET devices on a substrate, ~10 nm of insulating Al_2O_3 layer was deposited via the atomic layer deposition (ALD) method to serve as the isolation and gate oxide layer. For the macroscopic piezoelectric effect, a single-crystalline ZnO PFW with clean edges (see Figure 2B) was chosen for the device assembly. As for the piezoelectric hybrid FET, one end of a uniform ZnO wire was placed onto the SWNT channel perpendicular to the aligned SWNTs. The wire was unevenly placed to use the large piezopotential toward the end. The two ends of the ZnO wire were fixed by polyepoxide.

The practical structure of a fabricated FET is presented in Figure 2C,D. Highly doped silicon substrate with a 200 nm thick SiO_2 insulating layer was utilized as the back-gate for the SWNT channel (Figure 2C), while a ZnO PFW was utilized as the piezopotential gate for the SWNT channel (Figure 2D). Figure 2E shows the SEM image of a fabricated conventional FET structure on SiO_2 substrate. SWNTs clearly connected the drain−source electrodes and maintained their alignments. Figure 2F shows an optical micrograph image of the ZnO PFW gated hybrid device. In comparison to the gap between drain and source electrodes of ~2 μm, a relatively larger diameter ZnO PFW preferably gives an effective gating effect on both SWNT channels and metal contact areas. An atomic force microscopy image of the inside of the SWNTs on Kapton substrate is shown in Figure 2G, which was taken before the ALD process for the Al_2O_3 insulating layer. Most of the transferred SWNTs on both silicon and Kapton substrates exhibited their original alignments. Owing to the perpendicular alignment of SWNTs to the potential stretching axis of the ZnO wire, the strain effect on SWNTs can be safely neglected.

First, we have investigated the electric characteristics of SWNT FETs on silicon substrate as a quantitative reference for the piezopotential gated hybrid FETs. High-quality semiconducting SWNTs were employed here, which were produced utilizing Cu particles and methanol in a growth procedure.[20,21] We also have selected the devices with relatively lower *on* current ($\ll 1\ \mu A$), which is known to be proper for FET behavior in the SWNT device with multiple connections.[22] Semiconducting SWNT-based devices commonly show p-type behavior in ambient air due to trapped electron carriers by oxygen between SWNTs and metal contact area.[23] However, by capping SWNT FETs with an insulating layer from the ambient air environment, parasitic oxygen charge trap can be recovered, which allowed the devices to have both electron and hole carriers.[23,24] Figure 3A shows typical characteristics of the fabricated back-gated SWNT FETs on silicon substrate. After the deposition of top insulating Al_2O_3 layer, most of the fabricated SWNT FETs exhibited ambipolar behaviors as expected. Note that our FETs exhibited not only typical ambipolar behaviors but also a broad range of neutrality points from −5 to 5 V. A plausible explanation is that each FET comprises multiple SWNTs with various chiralities, which result in different electronic properties in each device,[25,26] and also different amounts of electrostatic charges are established between the SWNT and insulating layer during device fabrication. It should be noted that such broad range of neutrality points can affect signal outputs in a hybrid FET.

The gate electrode in the hybrid FET will be replaced by the ZnO PFW in the hybrid devices, which implies that a gate has only negative potential due to the screening effect of n-type charge carriers in the ZnO wire.[27] Therefore, the

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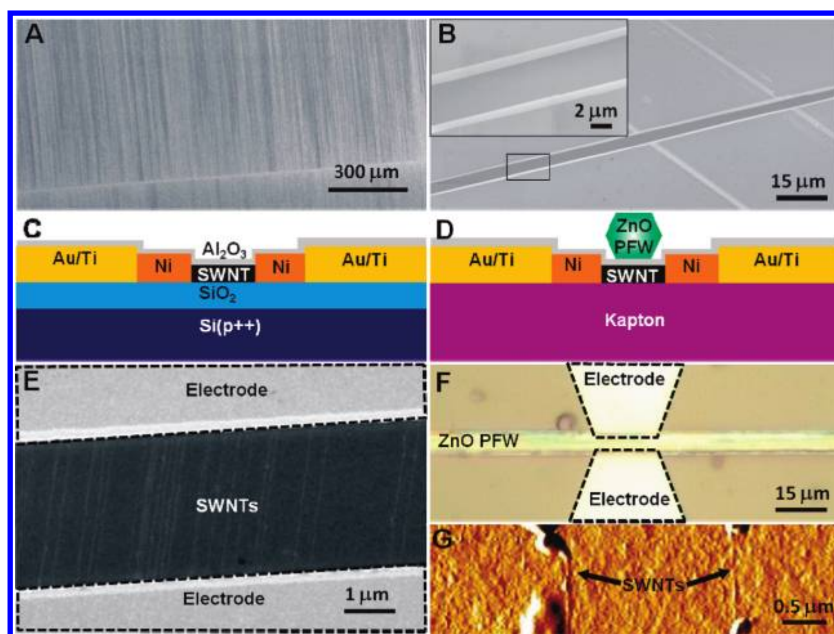

FIGURE 2. SEM images, optical images, and cross-sectional schemes for the fabricated FETs. (A) SEM image of well-aligned SWNTs on quartz substrate. SWNTs were grown from Cu nanoparticles with good alignment along the quartz substrate with single-crystal ST cut. (B) SEM image of the typical ZnO PFW. Inset shows the clean edge of the ZnO wire. (C) Schematic diagrams depicting the cross-section view of the SWNT FET on Si substrate. Highly doped silicon served as back-gate throughout electrical measurements. (D) Schematic diagrams depicting the cross-section view of a hybrid FET on Kapton substrate. Single-crystalline ZnO PFW served as a top gate without applying external electrical power. (E) SEM image of the SWNT junction on a SiO_2 substrate. Drain−source electrodes were clearly connected by well-aligned SWNTs. (F) Optical micrograph image of ZnO PFW gated hybrid FET on Kapton substrate. A relatively large PFW covered between the drain−source electrodes as the effective gate modulation to the SWNT channel and contact area. (G) Atomic force microscopy image of a SWNT junction underneath the ZnO PFW. Image was taken before the assembly of ZnO PFW on flexible Kapton substrate.

position of the neutrality points determines the direction of signal output in the hybrid FET. For example, the neutrality points positioned at negative gate voltage, V_G, area (red dots in Figure 3A) would show decreasing drain−source current; those positioned in positive area (green blocks in Figure 3A) would result in increasing behavior; the others in relative zero range (black blocks in Figure 3A) would have no change. The characteristics of neutrality points of the back-gated SWNT FET on a silicon substrate, transconductance, indicate potential types of signal outputs in a hybrid FET. For quantitative analysis, the transconductance ($\Delta I_{DS}/\Delta V_G$) around a zero gate voltage ($V_G = 0$ V) was plotted as a function of the initial drain−source current for the back-gated SWNT FET (Figure 3B). For a total of 26 SWNT FETs, the measured transconductance ranges from −20 to 20 nS due to their broad range of neutrality points, which can be classified into three groups, as displayed in Figure 3B: FETs with positive (≥+1 nS, red blocks in Figure 3A,B), negative (≤−1 nS, green blocks in Figure 3A,B), and nearly zero (<|1 nS|, black blocks in Figure 3A,B) transconductance. In our measurements of SWNT FETs on silicon substrate, the populations of FETs with positive, negative, and nearly zero transconductance were found to have a distribution of ∼38, ∼35, and ∼27%, respectively.

After characterizing the behaviors of the "strain-free" SWNT FETs under an externally applied gate voltage, we investigated their performance in the hybrid FET as the gate voltage being provided by the piezopotential of a ZnO PFW. Figure 3C presents a hybrid FET and the method for introducing a deformation in the ZnO PFW but not in SWNTs. By bending the Kapton substrate, the PFW follows the deformation of the substrate and generates a piezopotential drop along the wire. Since the thickness of the substrate was much larger than the diameter of the PFW, the applied stress is approximately along the *c*-axis of the ZnO PFW. The SWNT channel that was perpendicular to the *c*-axis of the PFW experienced negligible deformation. The drain−source current of the hybrid FET was continuously monitored when the PFW was bent and released periodically. Since an as-grown ZnO PFW is typically n-type, the electron carriers in the wire tend to largely screen the positive piezopotential at one end but leave almost no effect on the negative piezopotential side.[27]

In corresponding to the three groups of $I_{DS}-V_G$ characteristics in Figure 3A,B, three types of signal outputs were obtained utilizing the hybrid FETs (Figure 3D−F). By introducing a strain in the PFW via a periodic deformation of the substrate, the drain−source current for the hybrid FET shows a periodic decreasing, increasing, and no-change tendency, respectively, in corresponding to the three groups of FETs shown in Figure 3A. Because ZnO PFW generates effectively a negative gate voltage considering the n-type doping, and the piezopotential is usually less than −1 V, the hybrid FET with decreasing I_{DS} when the PFW was tensile

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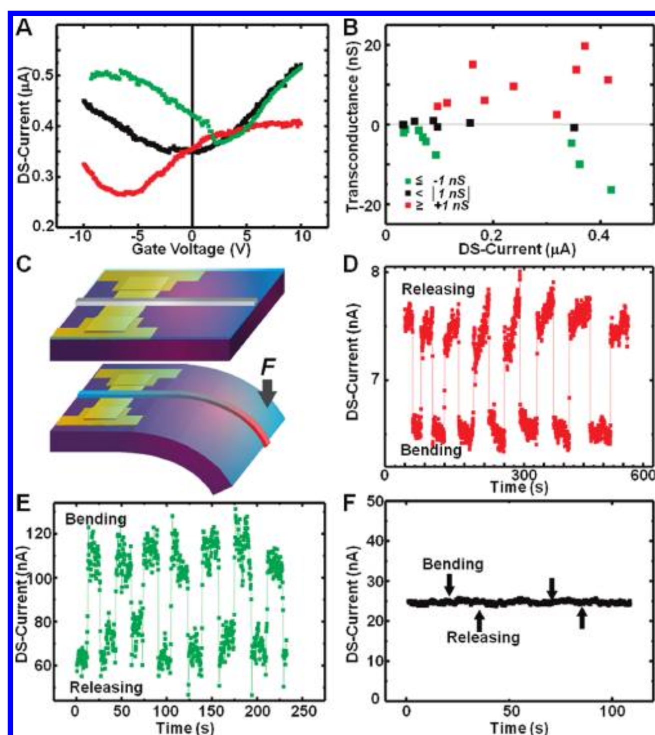

FIGURE 3. Gating effects of SWNT FETs through a Si back-gate and the ZnO PFW top-gate. (A) Typical three types of gating effects of the SWNT FETs on Si back-gated structure, which exhibits three different neutrality points. Red, green, and black rectangles represent negative, positive, and almost zero positions of neutrality points, respectively. (B) Transconductance distribution of SWNT FETs on a Si back-gated substrate around zero gate bias. Based on each value of transconductance (±1 nS), measured each device plotted with red (≥+1 nS), green (≤−1 nS), and black rectangles (<|1 nS|). (C) Schematic diagrams depicting the method for introducing a deformation in a ZnO PFW on a hybrid FET. Unevenly positioned ZnO PFW could modulate the electric field around the SWNT channel under stress. The external force was exerted by a micromanipulator positioned far away from the SWNT FET to reduce any coupled noise signal. Color represents the piezopotential drop along the ZnO PFW with red and blue representing positive and negative local piezopotential, respectively. (D) Response of a piezopotential gated hybrid FET to periodic bending deformation applied to the ZnO PFW. The increased gating effect is due to the SWNT FET with negative transconductance (red rectangles in panel B). Under the strain of 0.05%, the drain−source current, I_{DS}, of the hybrid FET increased from ~6.5 to ~7.5 nA. (E) Decreasing response of another piezoelectric gated hybrid FET to periodic bending deformation on the ZnO PFW. The decreased gating effect is due to the SWNT FET with positive transconductance (green rectangles in panel B). Under the strain of 0.05%, the drain−source current of hybrid FET increased from ~62 to ~118 nA. (F) Least response of a third type of piezoelectric gated hybrid FET to periodic bending deformation on the ZnO PFW. SWNT FETs with almost zero transconductance (black rectangles in panel B) corresponding to least gating effect.

stressed (Figure 3D) corresponds to the strain-free SWNT FET with positive transconductance (red rectangles in Figure 3B); the one with increased I_{DS} (Figure 3E) corresponds to the negative transconductance in the strain-free SWNT FET (green rectangles in Figure 3B). The percentage of drain−source current change ($\Delta I_{DS}/I_{DS}$) usually ranges from 10 to 40% for a strain of 0.05% (see also Figure S1 in Supporting Information). Furthermore, even when the strain increased from 0.05 to 0.1% with serial deformations, the drain−source current exhibited consequent changes (see Figure S2 in Supporting Information).

Furthermore, even under similar deformation, more than half of the fabricated FETs exhibited no appreciable response to the applied strain (Figure 3F), which cannot be explained as the case of strain-free SWNT FETs with small transconductance (black rectangles in Figure 3B). We will discuss such a case later. In all deformation steps, we evaluated the amount of strain in the ZnO PFW by utilizing Saint-Venant bending theory for small deflections (see Figure S3 in Supporting Information).[28,29]

To make our explanation concrete, both increasing/decreasing behaviors matched with direct gate performances using ZnO PFW as outside gate voltage. The magnitude of the piezopotential in our hybrid device can be directly quantified by comparing the amount of current change ΔI_{DS} of an FET when it is gated by piezopotential in reference to when it is gated by a top electrode (see Figure 4A). Since ZnO NWs have both piezoelectric and semiconducting properties, it can possibly be used as a gate electrode for FET, even if there is a potential drop due to the limited charge carrier in a ZnO wire.

At first, we used the ZnO PFW as a through path for outside gate voltage (Figure 4A, left-hand figure). In the measurement, the drain−source voltage bias V_{DS} was fixed at ~1 V, while outside gate voltage V_G through the ZnO wire (Figure 4A, left) was swept to modulate the drain−source current (red and green rectangles in Figure 4B,C).

Afterward, current change I_{DS} due to the piezopotential (black dot in Figure 4B,C) was also measured by applying an external deformation on the hybrid device but without applying a gate voltage (see Figure 4A, right-hand figure).

In Figure 4B, we first overlap plotted the two curves by matching the measured current change ΔI_{DS} for an FET with positive transconductance. $I_{DS}-V_G$ curve measured using outside gate voltage showed a behavior similar to that of strain-free FETs with positive transconductance (≥+1 nS, red blocks in Figure 3A,B). When the strain of 0.05% was applied along the ZnO PFW used for the same device, drain−source current decreased suddenly, which is plotted as a function of time in the same diagram. The piezopotential is directly received by examining the corresponding change in gate voltage of the FET when it was operated in conventional mode corresponding to the change of ΔI_{DS}, as shown by the dotted line in Figure 4B. The piezopotential for a strain of 0.05% is ~650 mV, which is smaller than the theoretically expected value without considering its finite conductivity (see Figure 1A). A plausible explanation could be the presence of defects in PFW, charge trap caused by ambient environment, or curvature mismatch between the substrate and the wire. We did the same measurement using a hybrid device with negative transconductance (Figure 4C), which showed increased current change when 0.05% strain was applied. In this case, the corresponding piezopotential

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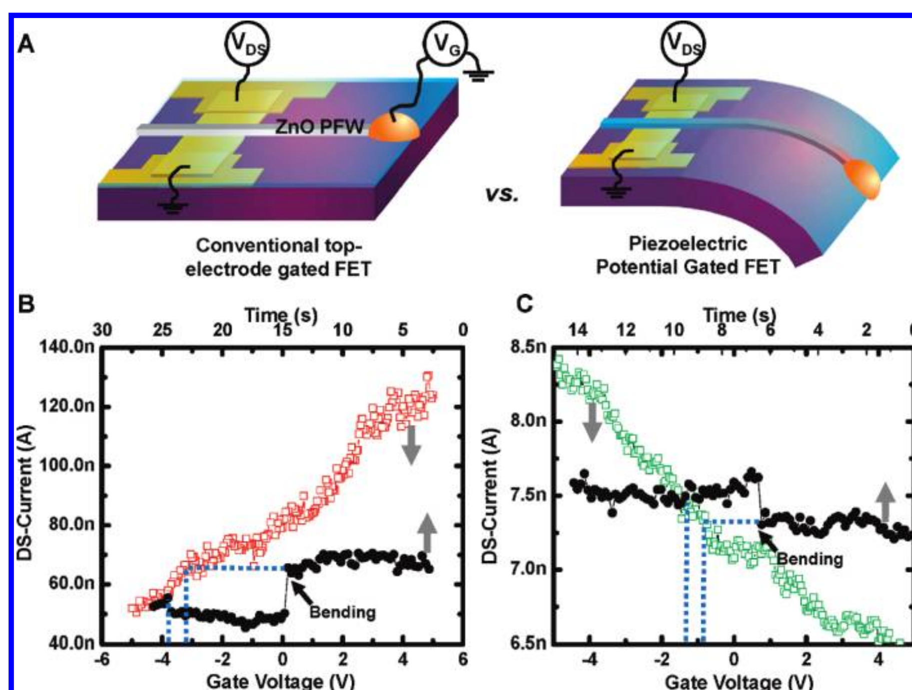

FIGURE 4. Quantifying the magnitude of the piezopotential in PFW. (A) Schematics of a carbon nanotube FET when it is gated by a conventional top electrode through the ZnO PFW (left-hand side) and when it is gated by the piezoelectric potential created by the PFW by straining (right-hand side). (B) Overlapped plot of a positive transconductance FET when it was operated in top electrode gated mode by swiping the gate voltage and when it was gated by piezopotential at a tensile strain of 0.05% (with on and off positions marked) as a function of time. (C) Same as (B) except for a negative transconductance FET.

created was ∼440 mV. This study shows a quantitative technique for measuring the piezopotential.

The polarity of the piezopotential is switched by reversing the strain from tensile to compressive,[30] the effect of which on the hybrid device has been studied. By changing the bending of the substrate from downward to upward (Figure 5A), the piezopotential in contacting with the SWNTs changes from negative to almost zero if the screening effect of the dopants to the positive piezopotential region is considered. Under tensile strain, the hybrid FET showed an abrupt response to straining (green rectangles in Figure 4B). On the other hand, almost no change was observed in the device under compressive strain (black rectangles in Figure 5B). This is because the positive piezopotential created in the PFW adjacent to the SWNT FET was largely screened by the n-type doping, which is equivalent to the case of absence of gate voltage.

We also carried out control experiments to rule out possible artifacts in device characterization. We replaced the single-crystal ZnO PFW with a polymer fiber coated with polycrystalline ZnO film. Because the coated layer was composed of randomly oriented ZnO nanocrystals, no macroscopic piezopotential would be produced regardless of the status of the strain. To rule out the possibility of SWNT FETs with small transconductance (<|1 nS|), we fabricated various control devices using polycrystalline ZnO as a gate, and all such devices exhibited constant currents even when there was an abrupt change of strain in the polycrystalline ZnO coated polymer fiber (see Figure S4 in Supporting Information). It implies that only macroscopic piezopotential generated in a single-crystalline fine wire can produce an effective gate bias to FETs nearby, just as expected. The residual strains in SWNTs and metal pads, if any, can cause only signal fluctuation in the noise level of the drain−source current.

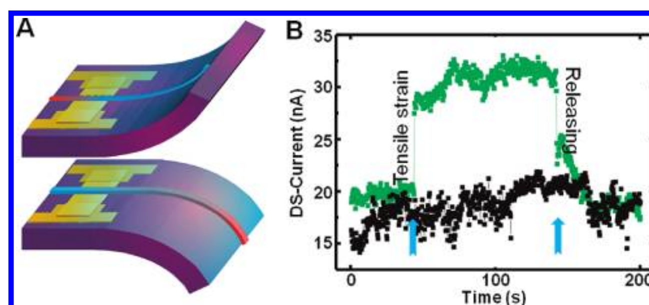

FIGURE 5. Effect of switching polarity of the piezopotential in a ZnO PFW on a hybrid FET. (A) Schematic diagram depicting a method for switching the piezopotential polarity in the ZnO PFW, as represented by the colored piezopotential drop along the wire, with red and blue representing the positive and negative local piezopotential, respectively. Owing to the screening effect of the n-type carriers in the ZnO PFW, the magnitude of the positive piezopotential is much reduced so that it has little effect on the carrier transport process, while the negative piezopotential is preserved. (B) Response of a hybrid FET on the switching polarity of the piezopotential in ZnO PFW. Green and black rectangles represent the drain−source current when the ZnO PFW was tensile and compressively strained, respectively. Only the tensile straining process in the PFW induces significant gating effect (green curve), while the compressive straining has little effect (black curve).

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Hybrid FETs with no response to strain were found to take more than half of the fabricated devices. Two possibilities may account for this statistical result: (1) The SWNT FET has almost zero transconductance (<|1 nS|) (black rectangles in Figure 3A,B), in which piezopotential was created and applied to the SWNT FET yet showed no response. (2) The side of the PFW in contact with SWNT has negligible positive piezopotential due to the screening effect of the n-type dopants. Since we could not control the $+c$-axis' crystallographic orientation in manipulating ZnO PFW during device assembly, there were equal possibilities to obtain negative and positive piezoelectric potential sides to be in contact with SWNTs. By including the SWNTs with almost zero transconductance, the hybrid FETs with no response to strain are expected to be more than ~50% of all devices fabricated.

In summary, we have demonstrated the first piezoelectric potential gated hybrid FETs based on nanotubes and nanowires. SWNT channel was fabricated on a flexible substrate utilizing a PMMA transfer method followed by a lift-off, deposition of insulating layer, as followed by an assembly of the crossed ZnO PFW. In the hybrid FET, SWNTs serve as a carrier transport channel, and a single-crystal ZnO PFW acts as the power-free and contact-free gate. The piezopotential created by an external force in the ZnO PFW is demonstrated to control the charge transport in the SWNT channel located underneath. This type of hybrid FET shows the first footstep toward gate-electrode-free and energy-harvesting FET. Furthermore, ZnO can be replaced by any piezoelectric materials for the hybrid FET as long as they can be made into single-crystalline wire shape, such as PZT and GaN. The force/pressure triggered hybrid FETs can be utilized as strain sensor, force/pressure sensor, security trigger, and analog-signal touch screen. Furthermore, piezoelectric potential gated hybrid FET could have the potential to be a multifunctional device system for a logic circuit, nanorobotics, NMES/MEMS, and self-energy generation.

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Supporting Information Available. Experimental details and additional figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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