Piezo-phototronic Boolean Logic and Computation Using Photon and Strain Dual-Gated Nanowire Transistors

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Emerging applications in wearable technology, pervasive computing, human–machine interfacing, implantable surgical instruments, and biomedical diagnostics[1] demand active and adaptive interactions between electronics and ambient/host (e.g., the human body). Direct detecting, processing, and control of the information encoded in environmental stimuli by logic units may therefore be necessary. Here we report implementation of piezo-phototronic binary computations, such as full addition and subtraction, over optical and mechanical dual-inputs through cascaded logic circuits in cadmium sulfide (CdS) nanowire (NW) networks. Using polarization charges created at metal–CdS interface under strain to gate/modulate electrical transport and optoelectronic processes of local charge carriers, the piezo-phototronic effect has been applied to design two-terminal transistors, which process mechanical and optical stimuli on the devices into electronic controlling signals. The NW networks have been further demonstrated for achieving gated D latch to store information carried by these stimuli. The piezo-phototronic logic devices may have applications in optical micro/nanoelectromechanical systems, tunable bio-optoelectronic probes, adaptive optical computing, and communication.

Piezoelectric effect has been widely used in electromechanical sensing, actuation, and energy harvesting, which produces polarization charges under mechanical deformation in materials lacking inversion symmetry or with polarization domains. Conventional piezoelectric materials such as $Pb(Zr_xTi_{1-x})O_3$ and poly(vinylidene fluoride) are insulators and not feasible for constructing functional electronics or optoelectronics. The effect of mechanically induced polarization on electronic and optoelectronic processes of charge carriers in piezoelectric materials has therefore been long overlooked. Recently, the three-way coupling among piezoelectric polarization, semiconductor properties, and optical excitation in wurtzite-structured piezoelectric semiconductors, such as ZnO and GaN, has resulted in both novel fundamental phenomena and unprecedented device characteristics as well as applications, leading to increasing research interests in the emerging field of piezo-phototronics.[2,3] For semiconductor materials with noncentral symmetry, piezoelectric polarization charges created upon straining can effectively tune/control the charge transport across interface/junction and modulate the optoelectronic processes of charge carriers, such as generation, separation, diffusion, and recombination. This is the piezo-phototronic effect.

CdS NW is of particular interest for investigating piezo-phototronic effect and implementing related applications, due to its visible range optical response and intrinsic piezoelectric property. CdS NWs used in this work were synthesized through a vapor–liquid–solid process (Experimental Section, Supporting Information).[4] A typical transmission electron microscopy (TEM) image of the as-synthesized NWs is shown in **Figure 1**a, indicating that the single-crystalline CdS NWs grow along [0001] direction (*c*-axis) and possess noncentrosymmetric wurtzite structure.[5] A single CdS NW was then transferred onto a poly(ethylene terephthalate) substrate for fabricating a flexible two-terminal metal–semiconductor–metal (M–S–M) device (Figure 1a and Figure S1, Supporting Information), with drain and source electrodes fabricated at the NW ends (Experimental Section, Supporting Information). Figure 1b shows the photoresponse of an as-fabricated device to visible light illumination with energy (wavelength = 442 nm) above the band gap of CdS (≈2.4 eV). When intensity of the illuminating laser exceeds a threshold value (≈50 mW cm^{-2}, Figure 1b inset), a significant enhancement in photocurrent (from 15.6 to 261 nA) is observed under moderate source bias, due to the photon generation of free carriers within the CdS NW (Figure 1e1).[6] The shape of photocurrent response is consistent with the formation of two back-to-back Schottky contacts between Ag electrodes and CdS NW, with Schottky barrier heights (SBHs) at both source and drain contacts lowered under photoexcitation (Figure 1e1).[7] Optical illumination with appropriate energy and intensity can therefore modulate the conductivity of the CdS NW device and turn it into electrically "on" state (Figure 1b inset).

Carrier transport in the CdS NW device can also be controlled by mechanical strain. Figure 1c shows the device's drain–source current in the dark condition as a function of applied strain (Figure S2 and S3, Supporting Information). The asymmetric trend observed in dark current at the source and drain electrodes in response to strains indicates the characteristics of the piezotronic effect,[2] which is the modulation of local interfacial band structure and charge carrier transport across junction/contact formed in piezoelectric semiconductor devices by strain-induced polarization charges at the interface. When a compressive strain is applied onto the CdS NW, positive, and negative piezoelectric polarization charges appear in the vicinity of Schottky barrier interfaces at the source and drain contacts, respectively, owing to the *c*-axis orientation of the wurtzite CdS NW (Figure 1a,e2).

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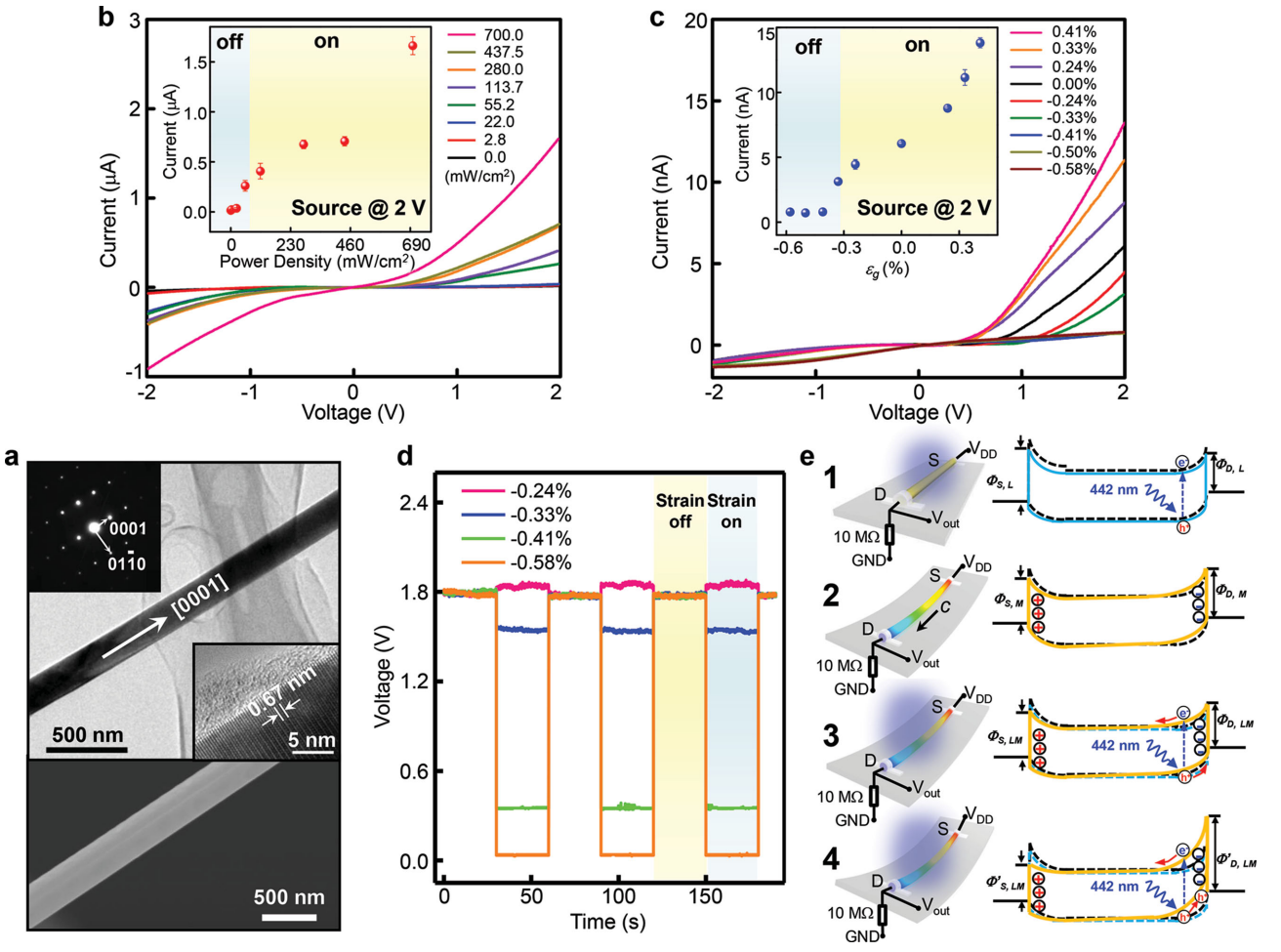

Figure 1. Characterization and working principle of light-strain dual-gated transistors (LSGTs). a) SEM, TEM, HRTEM, and corresponding selected area electron diffraction (SAED) pattern of a CdS NW. b) *I–V* characteristics of a typical LSGT under different light power densities of a 442 nm laser beam, a triangular wave swiping from –2 to 2 V was applied across the device. The inset shows a current versus power density curve with source electrode biased at 2 V. c) *I–V* characteristics of a typical LSGT under different strain conditions without light illumination, a triangular wave swiping from –2 to 2 V was applied across the device. The inset presents a current versus strain curve with source electrode biased at 2 V. d) *V–t* characteristics of a typical LSGT under 700 mW cm^{-2} illumination of a 442 nm laser beam, by applying four different strains periodically on the device. e) Schematic illustration of LSGTs and the corresponding band diagrams under (1) 442 nm laser illumination; (2) small compressive strains; (3) small compressive strain and 442 nm laser illumination; (4) large compressive strain and 442 nm laser illumination. Band diagrams under no laser illumination nor strains are presented by the black dashed lines in (1–4); under laser illumination, no strains are presented by blue solid lines in (1) and blue dashed lines in (3,4); under small compressive strains, no laser illumination are presented by yellow solid lines in (2); under small compressive strains and laser illumination are presented by yellow solid lines in (3); under large compressive strains and laser illumination are presented by yellow solid lines in (4).

Positive polarization charges attract the free electrons toward the barrier interface, giving rise to a reduced depletion width and therefore decreased local barrier heights at source contact; while the negative polarization charges repel the electrons away from the interface, resulting in a widened-depleted zone and thus increased local barrier heights at drain contact (Figure 1e2). Similarly, negative (positive) piezoelectric polarization charges induced at source (drain) barrier by applying tensile strains increase (decrease) the corresponding local SBHs. Since electronic transport in M–S–M structure is dictated by the contact with reversely biased Schottky barrier,[8] a change in SBH (calculated and shown in Figure S4, Supporting Information) at the reversely biased drain contact due to strain-induced polarization charges results in the observed transport curves in Figure 1c, showing a significant increase of current from 0.8 nA (at –0.58% strain) to 3.1 nA (at –0.33% strain), 6.1 nA (strain free) and 13.8 nA (at 0.41% strain) when source electrode is biased at 2 V. The mechanical strain hence effectively functions as the controlling gate signal in two-terminal CdS NW device (Figure 1c inset).

We have further studied the piezo-phototronic effect in two-terminal CdS NW device by introducing both optical illumination and mechanical strain to the device. A pull-down resistor (10 MΩ) is connected between the drain electrode and the ground. The voltage across the resistor is monitored when CdS NW is under different illuminations and strains (Experimental Section). For example, the output voltage under 700 mW cm^{-2} illumination increases from 1.8 to 1.85 V under –0.24% compressive strain, while the value decreases from 1.8 to 1.53 V,

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0.35 and 0.03 V when compressive strain further increases to –0.33%, –0.41%, and –0.58%, respectively (Figure 1d). The negative polarization charges-induced under small compressive strains (–0.24%) increases the local electric field intensity in the depletion region at the drain barrier. The modified band profile hence promotes the separation and mitigates the recombination of photoinduced electron-hole pairs by accelerating the drift of both charge carriers (Figure 1e3). Consequently, photoconductivity of the CdS NW device increases when small compressive strains are applied, as evidenced by the increase in output voltage across the pull-down resistor (Figure 1d, for the –0.24% strain case). When the applied compressive strain is high enough, however, the edge of the CdS NW's valence band at the interface is raised above the Fermi level of the electrode. As a result, an energy barrier for holes is formed at the drain barrier interface, which hinders the separation of photoinduced electron-hole pairs and promotes the recombination of them, with the photogenerated holes trapped at the drain barrier (Figure 1e4). The significantly increased SBH at reverse-biased drain barrier further reduces the photocurrent. Therefore, photoconductivity of the CdS NW device decreases when large-enough compressive strains are applied, as indicated by the decrease in output voltage (Figure 1d, for the –0.33%, –0.41%, and –0.58% strain cases). When the illumination intensity is low, on the other hand, separation of photoexcited electron-hole pairs is nearly complete. Change in device conductivity is therefore dominated by the change of band profiles at reversely biased drain barrier due to strain-induced polarization charges.[9] With less screening of the polarization charges by photoinduced free carriers under low-intensity illumination, the energy barrier for hole transport at drain barrier forms under even smaller compressive strains (Figure S5, Supporting Information). In consistence with this, output voltage across the pull-down resistor monotonically decreases with increasing the compressive strains in the CdS NW under low-intensity illuminations (Figure S5, Supporting Information).

Using polarization charges created at M–S interface under strain to gate/modulate electrical transport and optoelectronic processes of local charge carriers via the piezo-phototronic effect, we are therefore able to implement the shown two-terminal light-strain-gated transistor (LSGT), which processes mechanical and optical stimuli on the devices into electronic controlling signals (Figure 1d, Figure S5, Supporting Information). Significantly, these data demonstrate that two distinct states are observed with on/off ratio larger than 60. For example, after 700 mW cm^{-2} illumination is applied, conductance of LSGT changes by $\approx 10^3$ times as strain inputs vary between 0 ("strain off") and –0.58% ("strain on") (Figure 1d), with the output voltage switching from 1.8 to 0.03 V, respectively. We define the low resistance state as electrically "on" and the high resistance state as electrically "off" of the LSGT. This is different from the voltage-gated operation of traditional field effect transistor (FET). Neither of the above programmed state shows degradation over prolonged period (Figure S6, Supporting Information). The stable programmability of individual LGSTs between the "on" and "off" states allows further construction of distinct functional circuits from cascaded network of LGSTs as described below.

We first investigate the potential of these "dual-gate" programmable LSGTs for building fundamental logic gates with four coupled NW elements (**Figure 2** and Figure S7, Supporting Information). Each of these four LGSTs has two independently configurable gate-controlling signals, L_{in} and ε_{in}, for optical and mechanical inputs, respectively. The output from these logic units is electrical voltage. In our demonstration, the logic "0" state for optical input L_{in} is defined as focusing the 442 nm laser with intensity of 700 mW cm^{-2} on #2 and #4 LSGTs; the logic "1" state for optical input L_{in} is defined as focusing the 442 nm laser with intensity of 700 mW cm^{-2} on #1 and #3 LSGTs. The logic "0" state for mechanical input ε_{in} is defined as applying –0.58% compressive strains on #1 and #2 LSGTs; the logic "1" state for mechanical input ε_{in} is defined as applying –0.58% compressive strains on #3 and #4 LSGTs (Figure 2 and Figure S7, Supporting Information). These definitions are adopted in all demonstrations here and afterward. Figure 2a,d,g illustrate the configurations of piezo-phototronic AND, XOR, and OR logic gates comprising of four LGSTs. These piezo-phototronic logic operations are experimentally verified as shown in Figure 2b,e,h, with low electric output (logic "0" output) at around 0 V and high electric output (logic "1" output) at around 2 V, which is the bias voltage V_{DD}. The physical values of input and output signals are presented in the experimental truth table in Figure 2c,f, and i. Only the instances when both L_{in} and ε_{in} are logic "0" are illustrated in Figure 2a,d and g, which also highlight the distribution of piezoelectric polarizations. The complete operation schemes of these piezo-phototronic logic gates are explained in details in Supporting Information (Figure S8, Supporting Information). Other piezo-phototronic universal logic units, including NAND and NOR logic gates, were also successfully demonstrated (Figure S7, Supporting Information).

Piezo-phototronic arithmetic logic computations, such as one-bit half adder and subtractor have been further implemented by assembling the above fundamental logic gates with external wiring (**Figure 3**). The operation of piezo-phototronic half-adder is programmed as shown in Figure 3a by integrating XOR and AND logic units, which computes the summation of two inputs L_{in} and ε_{in}. The outputs SUM (S) and CAR (C) represent the sum and carry-out of the summation of the two inputs, respectively, with $S = L_{in} \oplus \varepsilon_{ir}$ and $C = L_{in} \cdot \varepsilon_{ir}$. The symbols "⊕" and "·" represent logical XOR and AND. Typical operations of the resulting circuit for V_{DD} = 2.0 V (Figure 3b) show that, as the input levels of L_{in} and ε_{in} are swept from logic state "0" to logic state "1", the outputs S and C switch between logic "0" (both ≈0 V) and logic "1" (2.0 and 1.99 V, respectively). Further tests show that the output of S and C for four typical input combinations (Figure 3b) all had similar output ranges: ≈0 V for logic state "0" and 1.9–2.0 V for logic state "1". The expected and experimental results for a piezo-phototronic half adder are summarized in the truth table (Figure 3c), which shows good consistency for this fundamental logic unit. By designing the wiring layout, piezo-phototronic half-subtractor has also been presented. The two outputs of the circuit, DIF (D) and BOR (B), represent the difference and borrow, respectively, of the subtraction of inputs $L_{in} - \varepsilon_{in}$, with $D = L_{in} \oplus \varepsilon_{ir}$ and $B = \overline{L_{in}} \cdot \varepsilon_{in}$, where $\overline{L_{in}}$ is the logical negation of L_{in}. Measurements of D and B for different input combinations (Figure 3e) show that the output voltage levels for logic state "0"

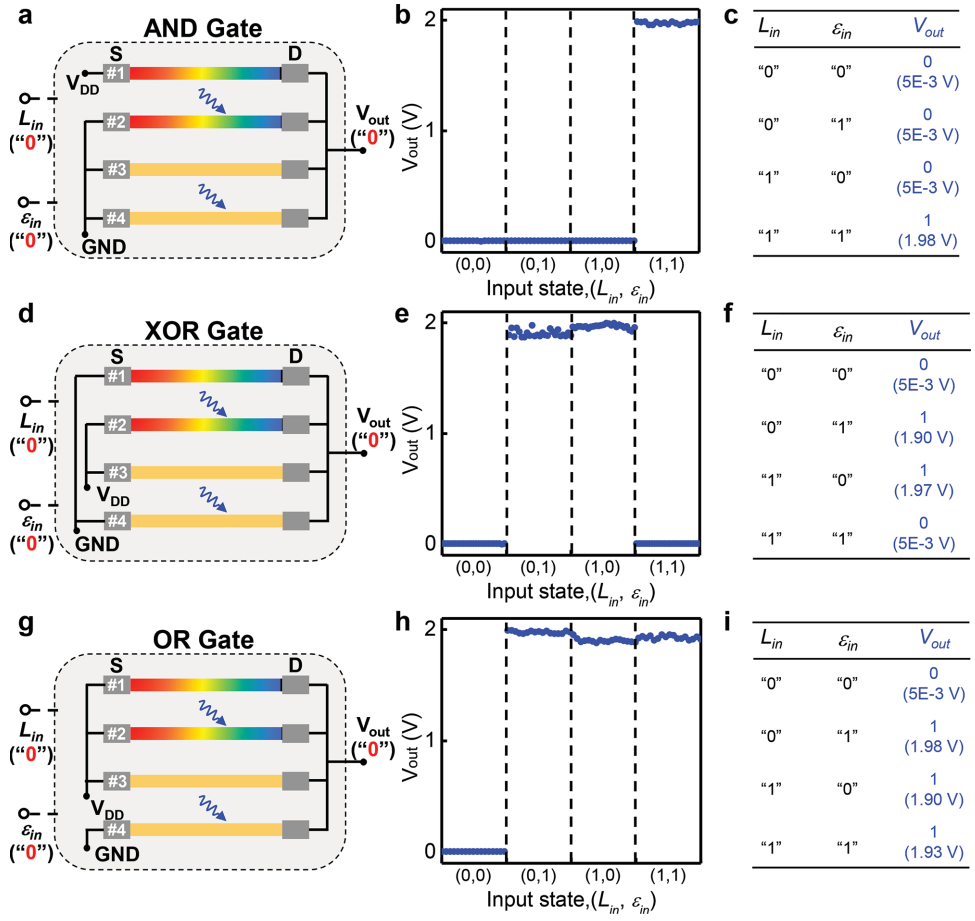

Figure 2. Light-strain-controlled piezo-phototronic logic gates and some basic operations. a–c) Piezo-phototronic logic AND gate. a) Schematic configuration of a piezo-phototronic logic AND gate comprising of four LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in the NWs highlighted using color code. b) Electric output signals of an AND gate under four input states as labeled, V_{DD} = 2 V. c) Experimental truth table with physical values of an AND gate. d–f) Piezo-phototronic logic XOR gate. d) Schematic configuration of a piezo-phototronic logic XOR gate comprising of four LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in NW highlighted. e) Electric output signals of a XOR gate under four input states as labeled, V_{DD} = 2 V. f) Experimental truth table with physical values of a XOR gate. g–i) Piezo-phototronic logic OR gate. g) Schematic configuration of a piezo-phototronic logic OR gate comprising of four LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in NW highlighted. h) Electric output signals of an OR gate under four input states as labeled, V_{DD} = 2 V. i) Experimental truth table with physical values of an OR gate.

(0.003–0.007 V) and logic state "1" (1.96–1.99 V) are well separated and represent robust states. Moreover, the truth table summarizing the expected and experimental results for the half subtractor (Figure 3f) shows consistent logic for this unit.

By introducing a third controlling signal, E_{in} for electrical input, to the cascaded network of LSGTs, more-complex piezo-phototronic units such as one-bit full adders and subtractors have also been demonstrated; these are important components for arithmetic logic operations in modern digital electronics. The experimental results show that these piezo-phototronic combinational circuits are capable of logically processing information carried by input signals from different domains through a set of Boolean functions. **Figure 4**a illustrates the configuration of a one-bit full-adder by cascading XOR and AND logic gates with specifically designed wiring layout, which computes the summation of three inputs, L_{in}, ε_{in}, and E_{in}. The outputs SUM (S) and CAR (C) represent the sum and carry-out of the summation of these three inputs, respectively, with $S = L_{in} \oplus \varepsilon_{in} \oplus E_{ir}$ and $C = (L_{in} \cdot \varepsilon_{in}) + (E_{in} \cdot (L_{in} \oplus \varepsilon_{in}))$. The symbols "⊕", "·", and "+" represent logical XOR, AND, and OR. Measurements of S and C for different input combinations (Figure 4b) show that the output voltage levels for logic state "0" (0.001–0.005 V) and logic state "1" (1.93–1.98 V) are well separated. The truth table summarizing the expected and experimental results for the full adder (Figure 4c) shows good consistency for this arithmetic logic unit. Similarly, operation of one-bit piezo-phototronic full-subtractor is realized (Figure 4d–f) for computing the subtraction of inputs $L_{in} - \varepsilon_{in} - E_{in}$, with $D = L_{in} \oplus \varepsilon_{ir} \oplus E_{in}$ and $B = E_{in} \cdot \overline{(L_{in} \oplus \varepsilon_{in})} + \overline{L_{in}} \cdot \varepsilon_{in}$, where $\overline{L_{in}}$ is the logical negation of L_{in}. Physical values of the outputs D and B are measured and summarized in Figure 4f,e, showing robust states as well as good consistency for this unit with output voltage levels for logic state "0" (0.001–0.005 V) and logic state "1" (1.90–1.98 V) well separated. The complete operation schemes of these

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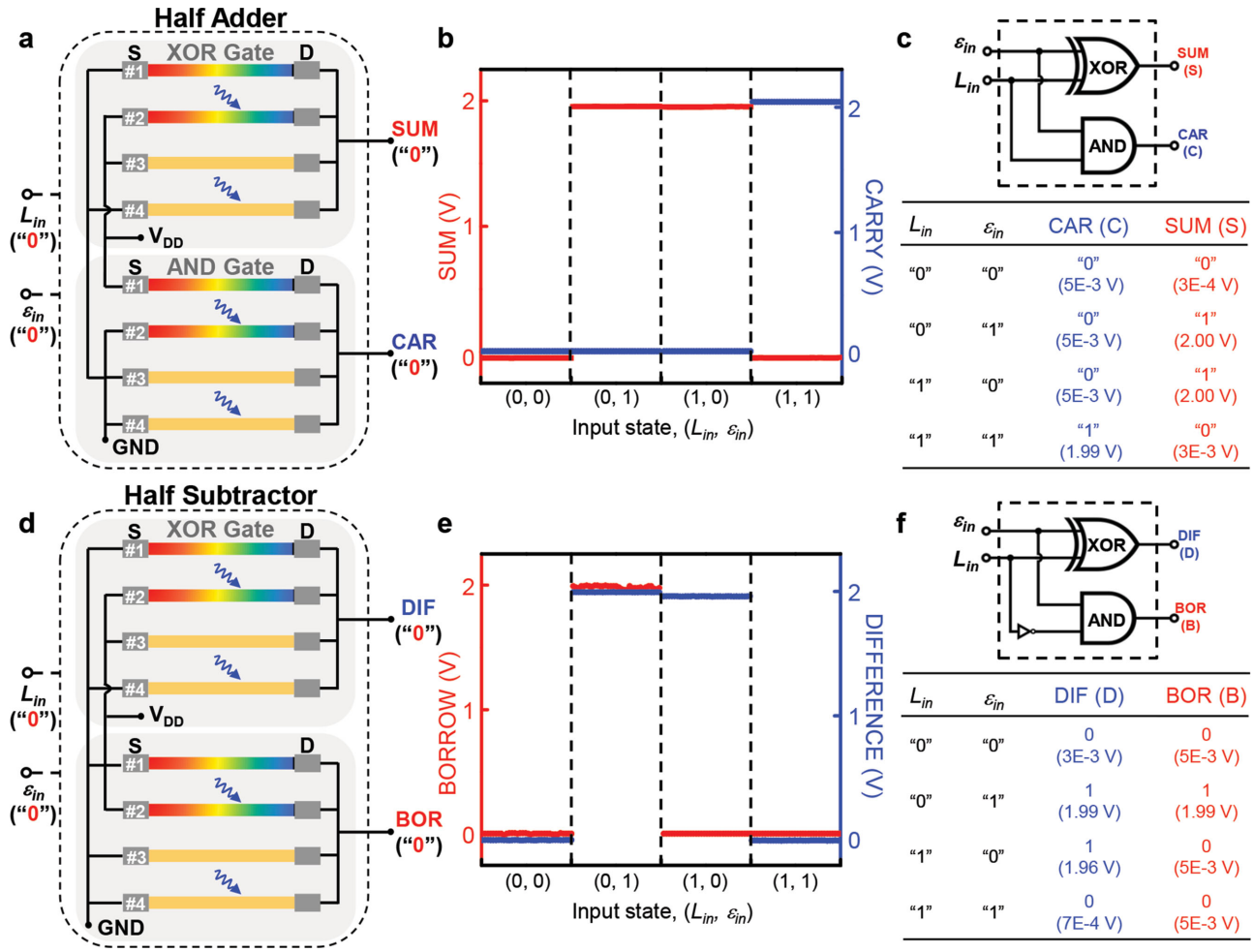
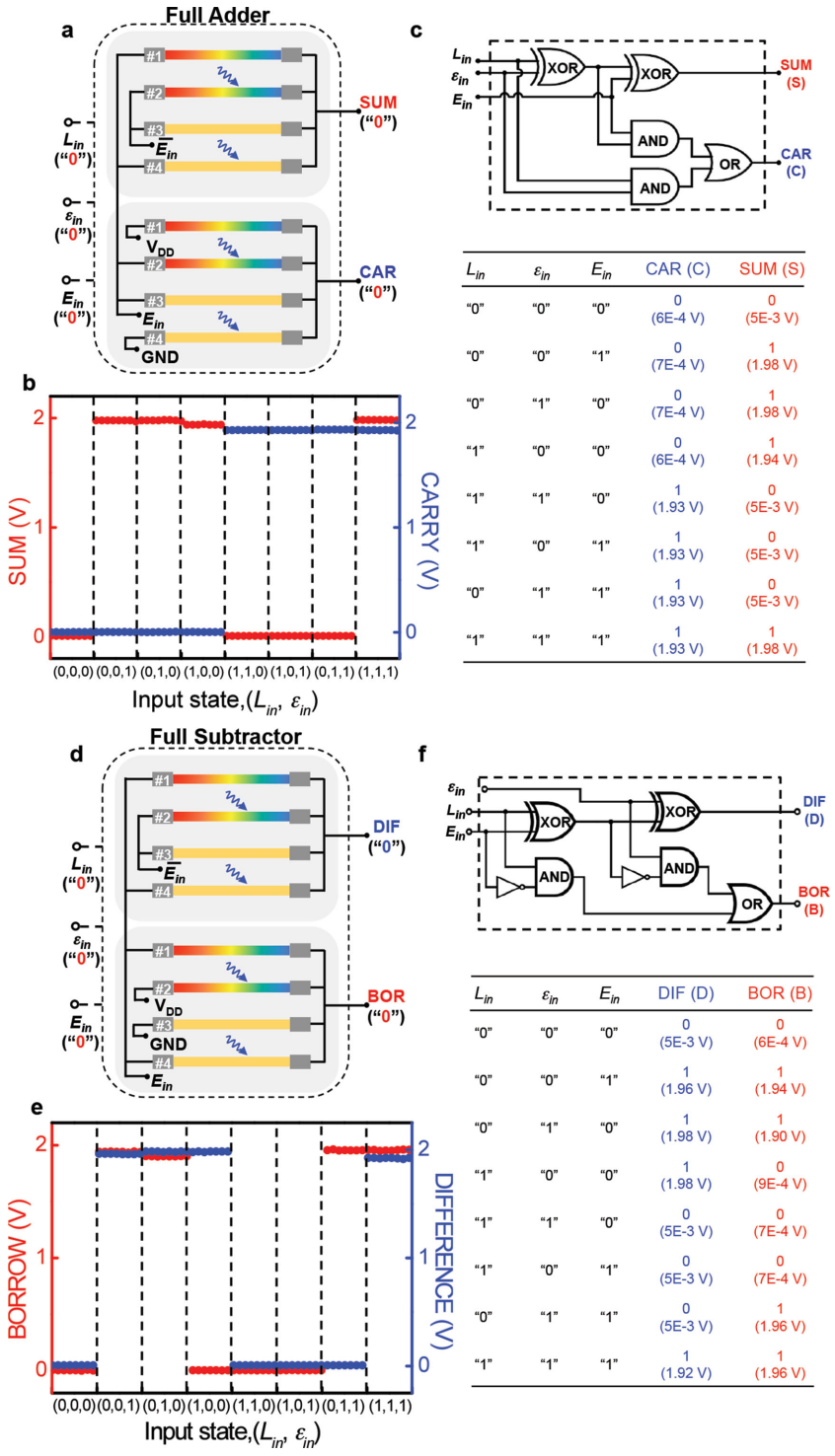


Figure 3. Light-strain-controlled piezo-phototronic logic computations. a–c) Piezo-phototronic half adder. a) Schematic configuration of a piezo-phototronic half adder comprising of eight LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in NW highlighted. b) Electric output signals of a half adder under four input states as labeled, V_{DD} = 2 V. c) Logic diagram and experimental truth table with physical values of a half adder. d–f) Piezo-phototronic half subtractor. d) Schematic configuration of a piezo-phototronic half subtractor comprising of eight LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in NW highlighted. e) Electric output signals of a half subtractor under four input states as labeled, V_{DD} = 2 V. f) Logic diagram and experimental truth table with physical values of a half subtractor.

piezo-phototronic combinational circuits are explained in detail in the Supporting Information (Figure S9 and S10, Supporting Information). These results show the capability and flexibility of the cascaded network of LSGTs to achieve the critical functions of combinational circuit elements, which also present the potential to integrate these prototype devices into even larger scale integrated circuits such as multibit arithmetic computations in an integrated configuration.

Notably, the assembled LSGTs units can also be configured as a sequential circuit element such as the D latch,[10] which represents an important component beyond the scope of combinational elements for information storage in digital circuits and communications. The outputs of D latch depend not only on the present inputs, but also on the states of memory elements (past inputs). **Figure 5**a shows the piezo-phototronic D-latch circuit composed of one LSGTs based NAND gate (I) and three conventional FETs-based NAND gates (II, III, and IV) with two feedback connections between output Q and input to NAND gate IV, as well as output $\overline{Q}$ and input to NAND gate III (Figure S11, Supporting Information). As a consequence, the output signal Q equals the input D (optical input, L_{in}) when the clock signal E (mechanical input, ε_{in}) is set to logic "1", but remains in its previous state if the clock signal E is set to logic "0". Both the optical and mechanical inputs here follow the universal definition mentioned previously. We applied 3 V to all the V_{DD} terminals labeled in Figure 5a to match input and output signal levels. Repetitive E and D inputs pulses were programmed to test the operation of piezo-phototronic D latch, by applying strains and turning on laser beams periodically to the devices. The measured output Q (Figure 5b, left) clearly followed the input data D when E was switched to logic "1" (–0.58% compressive strains on #3 and #4 LSGTs), and retained its previous value when the clock E was set to logic "0" (–0.58% compressive strains on #1 and #2 LSGTs). A second



L_{in}	ε_{in}	E_{in}	CAR (C)	SUM (S)
"0"	"0"	"0"	0 (6E-4 V)	0 (5E-3 V)
"0"	"0"	"1"	0 (7E-4 V)	1 (1.98 V)
"0"	"1"	"0"	0 (7E-4 V)	1 (1.98 V)
"1"	"0"	"0"	0 (6E-4 V)	1 (1.94 V)
"1"	"1"	"0"	1 (1.93 V)	0 (5E-3 V)
"1"	"0"	"1"	1 (1.93 V)	0 (5E-3 V)
"0"	"1"	"1"	1 (1.93 V)	0 (5E-3 V)
"1"	"1"	"1"	1 (1.93 V)	1 (1.98 V)

L_{in}	ε_{in}	E_{in}	DIF (D)	BOR (B)
"0"	"0"	"0"	0 (5E-3 V)	0 (6E-4 V)
"0"	"0"	"1"	1 (1.96 V)	1 (1.94 V)
"0"	"1"	"0"	1 (1.98 V)	1 (1.90 V)
"1"	"0"	"0"	1 (1.98 V)	0 (9E-4 V)
"1"	"1"	"0"	0 (5E-3 V)	0 (7E-4 V)
"1"	"0"	"1"	0 (5E-3 V)	0 (7E-4 V)
"0"	"1"	"1"	0 (5E-3 V)	1 (1.96 V)
"1"	"1"	"1"	1 (1.92 V)	1 (1.96 V)

Figure 4. Light-strain-controlled piezo-phototronic combinational logic circuits. a–c) Piezo-phototronic one-bit full adder. a) Schematic configuration of a piezo-phototronic one-bit full adder comprising of eight LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution in NW highlighted. b) Electric output signals of a one-bit full adder under eight input states as labeled, V_{DD} = 2 V. c) Logic diagram and experimental truth table with physical values of a one-bit full adder. Electric inputs E_{in} follows the conventional definition, logic "0" state is defined as low voltage, logic "1" state is defined as high voltage. d–f) Piezo-phototronic one-bit full subtractor. d) Schematic configuration of a piezo-phototronic one-bit full subtractor comprising of eight LSGTs, taking optical and mechanical inputs combination (0, 0) as a demonstration with piezo-potential distribution highlighted. e) Electric output signals of a one-bit full subtractor under eight input states as labeled, V_{DD} = 2 V. f) Logic diagram and experimental truth table with physical values of a one-bit full subtractor.

input waveform was designed to confirm the robust operation of this piezo-phototronic sequential logic circuit (Figure 5b, right). The corresponding truth table summarizing the expected and experimental results as well as comments for the D latch are shown in Figure 5c, with good consistency of the logic. These results suggest that the demonstrated piezo-phototronic D latch can process and store the information carried by external stimuli, such as mechanical strains and optical illumination.

Our LSGTs and cascaded piezo-phototronic circuits possess novel, unique, and complement features in comparison with existing electronics circuits based on top-down or bottom-up approaches.[11,12] First, the demonstrated design and results are different from the electrically gated FET, by replacing the external gating voltage with strain-induced polarization charges for controlling transport and other optoelectronic processes of charge carriers through the piezo-phototronic effect. This is a fundamentally new mechanism that enables the multifunctionality of assembled devices complementary to standard electrical operations realized using thin-film semiconductors and nanomaterials.[10,11,13] Second, the presented piezo-phototronic device eliminates the gate electrode and offers a new approach for 3D structuring and integration. The structural transformation from three-terminal configuration into two-terminal one may significantly simplify the layout design and circuitry fabrication for high density device while maintaining effective control over individual devices. Third, the direct processing and storage of information carried by external stimuli other than electrical signals by piezo-phototronic circuits, which is not available in existing technologies, provides great versatility and potential for developing tunable/adaptive electronics and optoelectronics to carry out intelligence-bearing interactions with the ambient environment.[14] The electronic output signals from piezo-phototronic circuits after processing the encoded information in ambient stimuli may make possible the control of embedded electronics and sensors for intelligent and adaptive operations in human–electronics interfacing,

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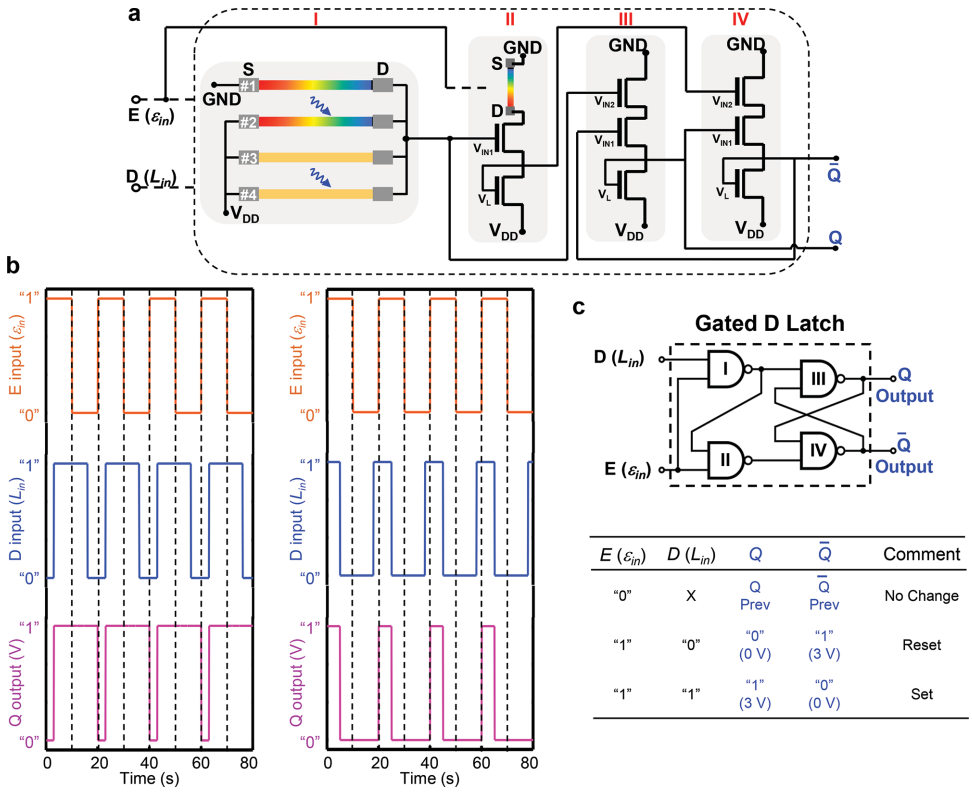

E (ε_{in})	D (L_{in})	Q	$\bar{Q}$	Comment
"0"	X	Q Prev	$\bar{Q}$ Prev	No Change
"1"	"0"	"0" (0 V)	"1" (3 V)	Reset
"1"	"1"	"1" (3 V)	"0" (0 V)	Set

Figure 5. Light-strain controlled piezo-phototronic sequential logic circuits. Piezo-phototronic gated D latch. a) Schematic configuration of a piezo-phototronic gated D latch composing of four NAND gates labeled as "I", "II", "III", and "IV". b) Two sets electric output signals of a gated D latch, output Q follows input data D when clock signal E is set to logic "1"; output Q retains its previous state when clock signal E is set to logic "0", V_{DD} = 3 V. c) Logic diagram and experimental truth table with physical values of a gated D latch.

optical micro- and nanoelectromechanical systems, bioprobes, and therapeutic devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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