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Strain-Gated Field Effect Transistor of a MoS_2–ZnO 2D–1D Hybrid Structure

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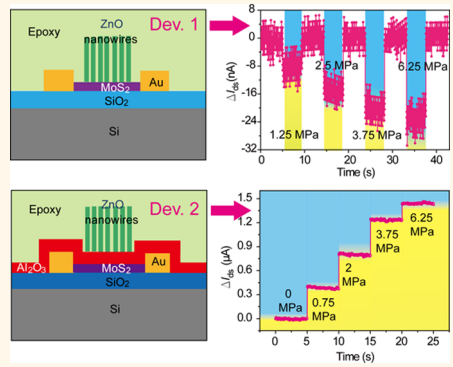
Supporting Information

ABSTRACT: Two-dimensional (2D) molybdenum disulfide (MoS_2) is an exciting material due to its unique electrical, optical, and piezoelectric properties. Owing to an intrinsic band gap of 1.2–1.9 eV, monolayer or a-few-layer MoS_2 is used for fabricating field effect transistors (FETs) with high electron mobility and on/off ratio. However, the traditional FETs are controlled by an externally supplied gate voltage, which may not be sensitive enough to directly interface with a mechanical stimulus for applications in electronic skin. Here we report a type of top-pressure/force-gated field effect transistors (PGFETs) based on a hybrid structure of a 2D MoS_2 flake and 1D ZnO nanowire (NW) array. Once an external pressure is applied, the piezoelectric polarization charges created at the tips of ZnO NWs grown on MoS_2 act as a gate voltage to tune/control the source–drain transport property in MoS_2. At a 6.25 MPa applied stimulus on a packaged device, the source–drain current can be tuned for ~25%, equivalent to the results of applying an extra −5 V back gate voltage. Another type of PGFET with a dielectric layer (Al_2O_3) sandwiched between MoS_2 and ZnO also shows consistent results. A theoretical model is proposed to interpret the received data. This study sets the foundation for applying the 2D material-based FETs in the field of artificial intelligence.



KEYWORDS: *strain/pressure, field effect transistors, MoS_2, ZnO, piezotronic effect*

MoS_2, as a member of the 2D transition-metal dichalcogenide material system, has unique electrical, optical, and piezoelectric properties[1−10] and can be exfoliated into monolayer or few-layer flakes.[11−13] Each 2D MoS_2 layer possesses three atomic layers of 6.5 Å thickness, where the molybdenum atom plane is sandwiched between two planes of sulfur atoms with the covalently bonded S–Mo–S atoms in a commonly found hexagonal-structured crystal.[14] Monolayer MoS_2 is confirmed to have a direct intrinsic band gap of ~1.85 eV and will change to an indirect band gap of 1.2 eV with layers increased to bulk.[14−16] Combined with a high-quality dielectric layer, monolayer or few-layer ultrathin MoS_2 field effect transistors (FETs) have been demonstrated with high mobility (>200 $cm^2\ V^{-1}\ s^{-1}$) and on/off ratio (~108),[1] near-ideal subthreshold swing (~70 mV per decade), and large current saturation window.[2,17]

FETs, as a basic component of modern electronics, are based on a fundamental principle that the source–drain current is gated by an applied voltage tuning the channel width.[18] A silicon-based FET has to be integrated with a capacitor or a piezoelectric layer in order to sense an externally applied mechanical stimulus.[19,20] Recently, piezoelectric semiconductor materials, such as ZnO, GaN, and CdS, are reported as excellent choices to fabricate smart devices with functions of sensitively detecting an external mechanical stimulus and simultaneously converting this stimulus to electrical signals.[21−25] Here we present a pressure-gated FET (PGFET) using a hybrid structure of a 2D MoS_2 flake and a 1D ZnO nanowire (NW) array.

RESULTS AND DISCUSSION

Single- or few-layer MoS_2 flakes were exfoliated from bulk MoS_2 and directly attached on highly doped p-type silicon substrates covered with 300 nm thick SiO_2, which is optimum for optical detection of MoS_2 flakes. Electrical contacts were patterned on MoS_2 flakes using lithography followed by successive deposition of Cr and Au. The precise location and region where the ZnO NW array would be grown at low temperature were defined by electron beam lithography, which guaranteed that ZnO NWs on the top of the MoS_2 flake were isolated from the source and drain electrodes (for more details see Supplementary Figure 1a). A schematic diagram and the

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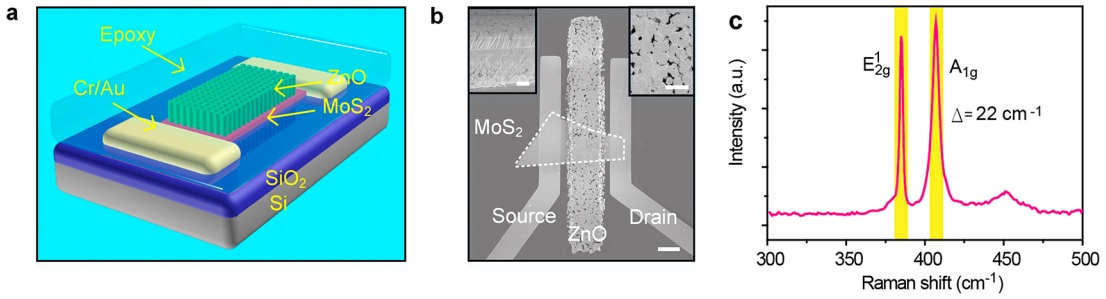

Figure 1. Device structure and characterization of ZnO NWs and MoS_2 flake. (a) Schematic illustration of a FET based on a MoS_2 and ZnO heterostructure. Using electron beam lithography, a small gap between source and drain electrodes was created, in which the ZnO nanowires were grown. (b) SEM images of the device before coating an epoxy layer for packaging. Inset: Enlarged side-view (left-hand) and top-view (right-hand) of the synthesized ZnO NW array. Scale bar: 3 μm in the large image and 1 μm in the inset images. (c) Raman spectrum of the MoS_2 flake used in this device.

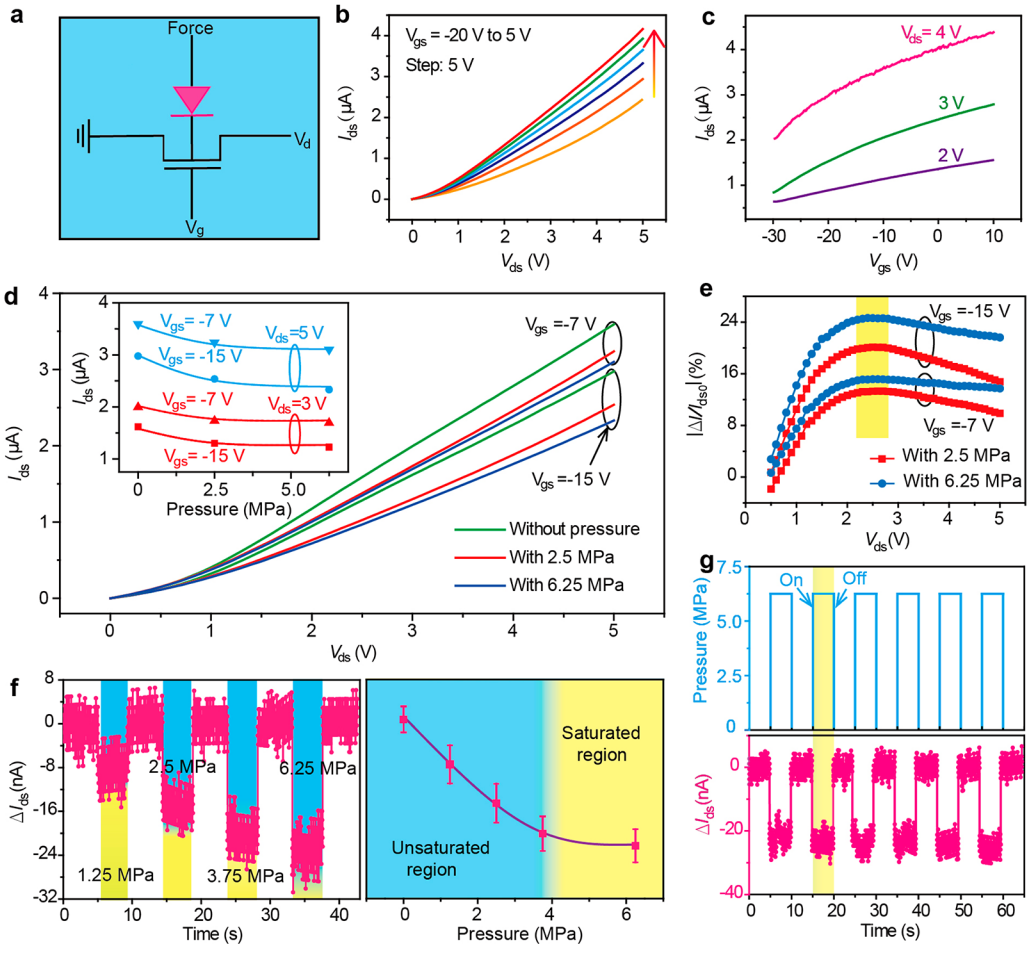

Figure 2. Response of the pressure-gated FET based on the MoS_2–ZnO heterostructure (Dev. 1). (a) Equivalent electrical circuit of the device. The heterostructure between the MoS_2 flake and ZnO NWs is represented by a diode. The characterizations of back gate electrically controlled FET: I_{ds}–V_{ds} output curves (b) and I_{ds}–V_{gs} transfer curves (c). (d) Pressure's modulation on the output curves of Dev. 1. The piezopotential of the ZnO NWs induced by the external stimulus acts as a gate voltage. Inset: Quantitative characterization of pressure *versus* drain current (I_{ds}). (e) Relative change in source–drain current derived from (d). I_{ds0} represents the drain current without applied pressure. Almost ~25% drain current change is obtained at the point of ~2.5 V drain voltage under the pressure of 6.25 MPa and gate voltage of −15 V. (f) Pressure-dependent change in drain current occurs at a bias voltage of 0.5 V drain and 0 V gate. Right-hand inset: Change in drain current plotted *versus* applied pressure, which shows that a linear variation of drain current *versus* pressure will reach saturation when the pressure is more than 4 MPa. (g) Observed change in drain current by periodically applying pressure to the device at the same bias voltage in (f).

corresponding practical device image (Dev. 1) are shown in Figure 1a and b. A layer of epoxy was used to encapsulate the entire device to keep its stability, which of course increased the strain required to generate the desired gating effect. The channel between the source and drain electrodes is about 7 μm, among which the ZnO NWs were grown *via* solution chemistry nearly perpendicularly to the substrate without contact with either electrode. This heterostructure of 2D MoS_2-contacted

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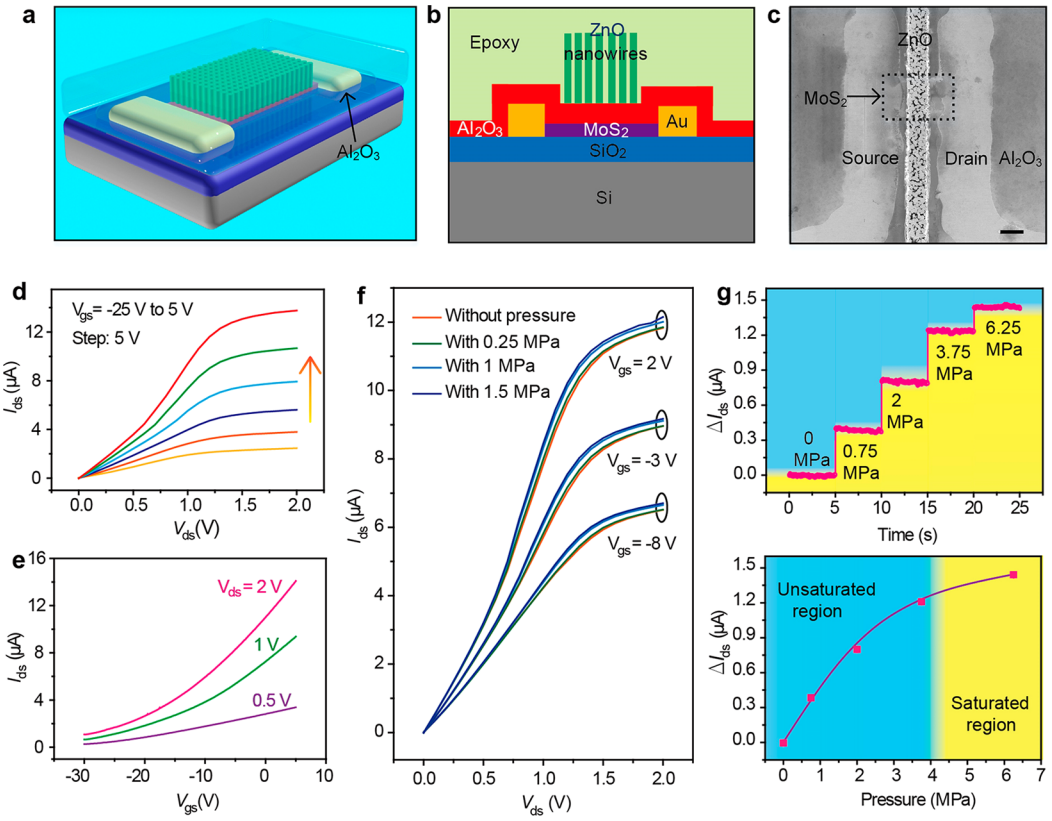

Figure 3. Response of the pressure-gated FET with an Al_2O_3 insulator layer sandwiched between MoS_2 and ZnO (Dev. 2). (a and b) Schematic cartoon graphs of the architecture of Dev. 2. The ZnO NW array and MoS_2 flake are separated by a 20 nm ALD-deposited Al_2O_3 layer. (c) SEM image of our practical device. Scale bar: 3 μm. I_{ds}–V_{ds} output (d) and I_{ds}–V_{gs} transfer characteristics (e) of the electrically controlled Dev. 2. (f) Response of the pressure-gated FET based on a MoS_2–Al_2O_3–ZnO hybrid structure under different gate voltages. With the pressure increasing, the drain current exhibits an increasing trend. (g) Pressure-dependent change in drain current at the drain voltage of 1 V and gate voltage of 2 V. Bottom inset: Plot of ΔI_{ds} with an increase in applied pressure. A saturated region appears when the pressure is more than 4 MPa.

1D ZnO NWs allows the piezopotential of the ZnO NWs, induced by the externally applied mechanical stimulus, to act as a gate to modulate the FET output. Before device fabrication, Raman characterization is employed to identify the thickness of the MoS_2 flakes (Supplementary Figure 2).[26,27] The Raman spectrum (Figure 1c) shows that the distance between the in-plane $E_{2g}{}^1$ mode and out-of-plane A_{1g} mode is 22 cm^{-1}, which confirms that the MoS_2 flake used for Dev. 1 was three layers.[28]

The equivalent electrical circuit of Dev. 1 is illustrated in Figure 2a. We define the heterostructure of MoS_2–ZnO as a diode, whose turn-on voltage is positive. The electrical characterization of the devices was performed at room temperature using a shielded probe station and a semiconductor parameter analyzer. The external pressure was applied by a digital force gauge (Supplementary Figure 3). All measurements were carried out in the dark because visible light can significantly increase the device's drain current due to the photoelectrical effect of MoS_2. We first characterized the back gate electrically controlled response of the MoS_2 heterostructure FET by applying a bias voltage to the drain and step voltage to a highly doped p-type silicon substrate with the source grounded as indicated in Figure 2a. The typical output and transfer characteristics are presented in Figure 2b and c, respectively. The I_{ds}–V_{ds} output curves increase when the gate voltage is increased owing to the free electron accumulation in the MoS_2 channel. This indicates that the semiconducting MoS_2 used here is an n-type,[2] which is the case for all fabricated devices regardless of the number of MoS_2 layers. We note that, compared with the MoS_2 FETs, the overall performance of the heterostructure FETs based on MoS_2–ZnO was degraded by the solution process for synthesizing ZnO NWs (Supplementary Figure 4).

Then we characterized the pressure-controlled response of Dev. 1 as systematically interpreted in Figure 2d–g. From the pressure-dependent output curves (Figure 2d), it is observed that increasing the pressure gives rise to a steadily decreasing drain current in spite of a different gate voltage. The inset exhibits that the decreasing trend could reach saturation, as demonstrated previously,[22] with the pressure increased under different drain bias voltages and gate step voltages. A relative change of drain current as shown in Figure 2e is defined as $|\Delta I/I_{dso}|$, where I_{dso} represents the drain current without applying pressure and ΔI is the change in current after applying pressure. Notably, a maximum peak for about 25% occurs at ∼2.5 V when the external pressure is fixed at 6.25 MPa and the gate voltage at −15 V, which is equivalent to the result of applying an additional ∼−5 V back gate voltage. Figure 2f presents the pressure-dependent change in drain current under a drain voltage of 0.5 V and gate voltage of 0 V. Externally applied pressure yields a piezopotential *via* ZnO NWs to modulate the output of the device, effectively acting as a back gate voltage. As the graph at the right-hand side of Figure 2f indicates, the change in drain current is almost linear to the applied pressure below ∼4 MPa and then reaches a saturated region.

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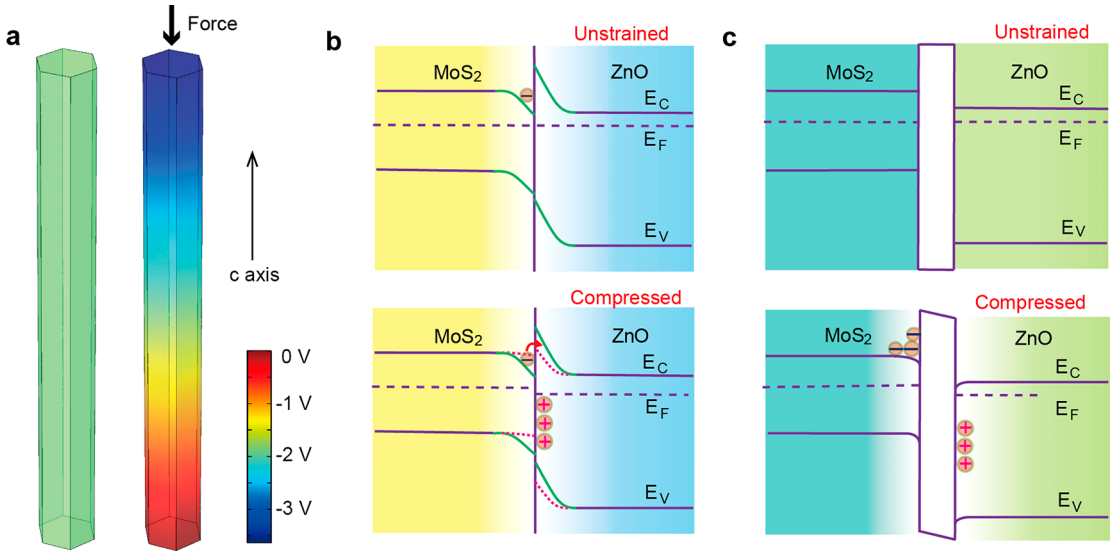

Figure 4. Schematic band diagrams to illustrate the underlying physical mechanism observed for the decreasing and increasing trends at an applied pressure for the two types of devices. (a) Piezopotential distributions in a ZnO nanowire (35 nm in length and 4 nm in diameter) under an axial force of 12 nN, simulated by a finite-element analysis method (COMSOL). (b) Energy bands of a MoS_2−ZnO heterostructure before (top) and after (bottom) applying a compressive force on ZnO NWs (Dev. 1). (c) Band diagrams of the MoS_2−Al_2O_3−ZnO structure before (top) and after (bottom) applying a pressure on ZnO (Dev. 2). See text for details.

Repeatability of the drain current variation at a periodically applied pressure of 6.25 MPa is shown in Figure 2g, exhibiting a good reproducibility.

Next, we developed another type of PGFET with a dielectric layer sandwiched between MoS_2 flakes and ZnO NWs (Dev. 2), which are schematically presented in Figure 3a and b. A 20 nm thick layer of high-quality Al_2O_3 was deposited on the as-fabricated MoS_2 FET using atomic layer deposition (Supplementary Figure 1b), which serves as an effective gate oxide. The orderly ZnO NW array is synthesized at the top of the Al_2O_3 layer shown in Figure 3c, under the same condition as for Dev. 1. The typical back gate electrically controlled characteristics of Dev. 2 are displayed in Figure 3d and e, respectively. The I_{ds}−V_{ds} transport exhibits linear behavior at low drain voltage and excellent current saturation at high drain voltage, which is a critical feature for both logic and analog circuits. When an external mechanical stimulus is applied, the piezopotential of the ZnO NWs serves as a gate voltage that controls the channel conductance. Figure 3f and g display the pressure-dependent output characteristics of Dev. 2. It is worth mentioning that the source−drain current gradually increases with the increasing of applied pressure, which is just opposite that of Dev. 1. The vertical structure of MoS_2−Al_2O_3−ZnO forms a typical capacitance like a traditional metal-oxide−semiconductor (MOS) structure. This significant feature distinguishes it from the FET based on a MoS_2−ZnO heterostructure and results in their exactly opposite response to external pressure, which will be discussed in detail later. The distinct pressure-controlled change in drain current of Dev. 2 is also clearly illustrated in the top graph of Figure 3g, where the variation of output current (ΔI_{ds}) is plotted as a function of time for different applied pressure to the local ZnO NWs. The gate voltage and drain voltage were fixed at 2 and 1 V, respectively, to achieve a large current variation (Supplementary Figure 5). The bottom graph shows quantitative characterization of the variation trend of pressure *versus* the change in drain current, where a saturated region also occurs when the pressure is more than ∼4 MPa.

Finally, we fabricated a series of FETs to reveal the underlying physical mechanism observed for the decreasing and increasing trends in Dev. 1 and Dev. 2, respectively. Five devices with the structure of Dev. 1 and five with the structure of Dev. 2 were tested, and all of them show consistent changes in source−drain current as presented above (Supplementary Figure 6). In this configuration, the transport characteristic change is attributed to two effects: a piezoresistance effect, which emphasizes the strain-induced band gap change, and a piezotronic effect, which is the strain-induced piezopotential modulation of the barrier height at the interface of the metal−semiconductor and p−n junctions.[22,29] To find out which dominates the devices, control experiments were conducted on the MoS_2 flake FET without ZnO NWs on the top (Supplementary Figure 4), which confirms that the piezoresistance effect and the piezotronic effect in the MoS_2 flake cannot produce the change in drain current for the hybridized structure. Therefore, the observed change in transport current for Dev. 1 and Dev. 2 when a pressure is applied can be caused only by the piezotronic effect of ZnO NWs on the MoS_2 flake.

According to the piezotronic theory,[30] we proposed a schematic band diagram to interpret the stated increasing and decreasing trends in Dev. 1 and Dev. 2 as shown in Figure 4. The piezopotential distribution in a ZnO NW under an applied force is simulated by a finite-element analysis method (COMSOL). When a force is applied on the nanowire, the superposition of the electric dipole moment along the *c*-axis generates negative and positive piezoelectric polarization charges (piezopotential) along the positive and negative *c*-axis, respectively, as indicated in Figure 4a. The as-synthesized ZnO NWs and the exfoliated MoS_2 flakes are all naturally n-type.[2,21] An n−n homotype heterojunction forms at the interface of these two semiconducting materials.[31] Due to the different work function and electron affinity between ZnO and MoS_2 (Supplementary Figure 7), electrons in the ZnO NWs may diffuse into the MoS_2 flakes at the junction area to balance the different Fermi levels as for Dev. 1, yielding a positively charged carrier (electron) depletion region on the ZnO side

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and a negatively charged carrier accumulation region on the MoS_2 side.[18] Under an equilibrium state, a barrier at the interface as shown in Figure 4b forms, which is of great significance to the modulation of the piezopotential on the channel current. Once pressure is applied on the ZnO NWs, the induced positive piezoelectric polarization charges in the depletion region lower the local barrier height,[30] leading to a redistribution of carriers at the junction region. Specifically, the mobile negative electrons in the MoS_2 conducting channel are attracted across the lowered barrier to screen the positive polarization charges on the ZnO side (Figure 4b); the reduced carrier concentration in MoS_2 decreases the drain current, as observed in Figure 2d.

Band diagrams of MoS_2−Al_2O_3−ZnO before (top) and after (bottom) applying an external pressure on Dev. 2 are illustrated in Figure 4c. Once a pressure is applied, the positive piezoelectric polarization charges are generated at the Al_2O_3−ZnO interface and electrostatically induce mobile electrons in the MoS_2 channel, similar to the case of traditional FETs gated by a back or top gate voltage. With increasing applied pressure, more free electrons are accumulated at the interface of MoS_2−Al_2O_3; accordingly the local carrier density is increased in the MoS_2 channel,[18] which yields an increase in source−drain current as indicated in Figure 3f and e. In brief, the positive piezoelectric charges in ZnO NWs accumulate mobile electrons in the MoS_2 channel by electrostatic induction in the structure of MoS_2−Al_2O_3−ZnO, while deplete free electrons from the MoS_2 channel in the structure of MoS_2−ZnO.

CONCLUSIONS

In conclusion, we have demonstrated external pressure-gated MoS_2 FETs, in which a few-layer MoS_2 flake acts as a conductive channel and piezoelectric ZnO NWs act as a gate triggered by local pressure. With respect to the specific structures, PGFETs can be divided into two groups: one corresponding to the FETs based on a MoS_2−ZnO heterojunction and the other corresponding to the FET based on a MoS_2−Al_2O_3−ZnO sandwich construction. When the applied pressure is increased, the decreasing and increasing change in source−drain current are respectively obtained for those two types of FETs. Finally, a corresponding theoretical model is presented. This work provides a technical route for fabricating piezoelectricity-controlled MoS_2 devices for flexible electronics and human−machine interfacing.

EXPERIMENTAL METHODS

Using the mechanical cleavage method as for graphene, a few-layer MoS_2 flake was exfoliated from bulk MoS_2 (SPI) on silicon substrates with 300 nm thick SiO_2. After UV-light or electron-beam lithography, Cr (5 nm, as adhesion layer) and Au (50 nm, as electrodes) were deposited using electron-beam evaporation. To fabricate Dev. 2, a 20 nm intermediate Al_2O_3 layer was deposited by atomic layer deposition at 200 °C for 40 min. Then the ZnO NWs were synthesized on the defined area of the as-fabricated MoS_2 FET (Dev. 1 or Dev. 2) in a nutrient solution containing 30 mM zinc nitrate hexahydrate and 30 mM hexamethylenetetramine at 80 °C for 4 h. Next, the FET was annealed at 200 °C for 2 h in a N_2 atmosphere to decrease contact resistance, improve the crystallinity of ZnO, and remove resist residue. Finally, the device was encapsulated by a layer of epoxy. All of the output or transfer curves were measured by a Keithley semiconductor parameter analyzer (4200).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b07121.

Device fabrication (Figure S1), Raman spectrum (Figure S2), optical graph of the testing platform (Figure S3), pressure's influence on the performance of a MoS_2 transistor without any hybrid structure (Figure S4), drain current change under different pressures and gate voltages as for Dev. 2 (Figure S5), histograms of change in drain current for two group devices at 2 MPa (Figure S6), electron affinity, work function, and band gaps of MoS_2 and ZnO used in the energy band diagrams (Figure S7) (PDF)

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Author Contributions

§L. Chen and F. Xue contributed equally.

Notes

The authors declare no competing financial interest.

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