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Theory of Tribotronics

*Ying Liu, Simiao Niu, and Zhong Lin Wang**

As a potential next generation mechanical-to-electricity power generator, the triboelectric nanogenerator (TENG) has drawn considerable attention in recent years. Its mechanical-to-electrical signal control properties also gave rise to the original idea of "tribotronics", which utilize triboelectric output to drive/control electronic devices. Using a TENG as input for gate voltage for a field effect transistor, a tribotronic device has potential application in mainly two areas (i) mechanically controlled electronics and (ii) motion/displacement sensing. An experimental study has already been recently reported and therefore a theoretical study is strongly desired as the theoretical basis and optimization strategy for designing such circuits. Here, both analytical calculations and numerical simulations are used to study the tribotronic device, both on the logic operation and on mechanical sensing. The static charge and inherent capacitance of TENG are determined by the structure design of the TENG and have strong coupling with the field effect transistor. Such coupling effect is taken into consideration, thus developing a methodology to effectively optimize the tribotronic device design according to such a coupling effect.

1. Introduction

The triboelectric nanogenerator (TENG) has drawn considerable attention in recent years, for its low material and processing cost and high energy conversion efficiency, making it potentially the next generation mechanical-to-electricity power generator with high total energy conversion efficiency (up to 80%), light weight and weight density and diversity applications.[1–3] On the other hand, its mechanical-to-electrical signal control properties also gives rise to the original idea of "tribotronics," which utilizes triboelectric output to control electronic devices, taking the role as a gate voltage as for conventional field effect transistor. As the first step, simple experimental demonstration has been reported recently, by using a contact mode attached-electrode TENG as input for gate voltage for a silicon based field effect transistor.[4,5] Such a device has potential application in mainly two areas, (i) mechanically controlled electronics and (ii) motion/displacement sensing.[6–11] Compared with previously proposed piezotronics,[12–14] in which the traditional externally applied gate voltage is replaced by the piezoelectric polarization charge created inner crystal potential, the tribotronics has easier physics mechanism and is also easily integrated into currently available silicon based circuits. Also, the tribotronics utilizes the potential created by triboelectric charges on the surface as a gate voltage to control the transport behavior. While the piezotronics utilizes the inner crystal piezoelectric potential created by piezoelectric polarization charges at the interface to control the charge transportation within the transistor. For mechanically controlled logic or mechanical sensing purposes, tribotronics possesses advantages including lower cost, easier control, and quick integration. However, as the nature of TENGs is related to static charges, and excessive static charges can lead to device breakdown in current semiconductor devices, the TENGs used for tribotronics should be carefully designed. Also, the inherent capacitance of TENG is usually small and comparable to the parasitic capacitance of metal-oxide-semiconductor field effect transistors (MOSFETs), so the coupling of TENG's output into logic circuit is also strongly affected by the structure design of the TENG.[15–20] Here we have used both analytical calculation and numerical simulation to study the tribotronic device, both on the logic operation and on mechanical sensing, providing the theoretical basis and optimization strategy for designing such kind of circuits.

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2. Logic Operation Realized by TENG

2.1. NMOS Inverter Gated by TENG

2.1.1. NMOS Inverter Basics

Logic operation is the first demonstration of the tribotronic devices. In such a device, the gate voltage of MOSFET is replaced by the output of TENG. To study the logic operation of tribotronics, we should first look into the properties of MOSFET and how it couples with the properties of TENG. In a conventional MOSFET, there are three electrodes for controlling its performance: the gate electrode **G**, source electrode **S**, and drain electrode **D**. The gate voltage V_{GS} controls the charge carrier channel between the source and drain electrodes. Depending on different applied drain voltage V_{DS} and gate voltage V_{GS}, for an ideal conventional long-channel MOSFET, there are three working regions, the off region, the linear region, and the saturation region. Depending on the applied gate electrode voltage and the drain electrode voltage, the current characteristic of the MOSFET varies.

We first take the most commonly utilized n-channel MOSFET (n-type metal-oxide-semiconductor (NMOS)) as an example. One of the most important parameters for a MOSFET is the threshold voltage V_T, which is intrinsically determined by the MOSFET itself:[21]

$$V_T = \left(\varphi_{ms} - \frac{Q_f}{C_{OX}}\right) + 2\psi_B + \frac{\sqrt{4\varepsilon_s q N_A \psi_B}}{C_{OX}} \quad (1)$$

where φ_{ms} is the work function between the gate material and the semiconductor, Q_f is the fixed oxide charges, C_{OX} is the capacitance of the oxide, N_A is the doping profile of the semiconductor, and ψ_B is the surface potential.

When the gate voltage $V_{GS} < V_T$, the conducting channel is closed, and the N-MOSFET is working at the off mode, the current flowing through the drain electrode to source I_D is zero.

When $V_{GS} > V_T$, an inversion layer is formed, and current from drain electrode to source electrode I_D begins to increase with increasing V_{DS}. When V_{DS} is small, the $I_D - V_{DS}$ relationship is linear, and MOSFET is working in the linear mode

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (2)$$

To simplify the result, the ratio constant of the NMOS is defined as $K_N = \mu_n C_{ox} W/2L$, thus Equation (2) is rewritten as

$$I_D = K_N[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (3)$$

When V_{DS} continues to increase and reaches the saturation point $V_{Dsat} = V_{GS} - V_T$, then I_D reaches a saturation value that is determined by V_{GS}, and MOSFET is working at the saturating mode

$$I_{Dsat} = K_N(V_{GS} - V_T)^2 \quad (4)$$

For tribotronic devices, a TENG is utilized to supply gate voltage. For the simplest case, we utilize a contact-mode attached-electrode TENG.[19] We assume the TENG is at steady state, and the inherent capacitance of the TENG C_{TENG} is much larger than the parasitic capacitance of MOSFETs so the inherent TENG capacitance is ignored. Therefore, the gate voltage now applied is the TENG open circuit voltage, as shown below.

$$V_{GS} = V_{OC} = \frac{\sigma x}{\varepsilon_0} \quad (5)$$

where σ is the surface charge density of the polymer used in TENG, x is the separation distance of the two surfaces in TENG, and ε_0 is the permittivity of vacuum space.

With this small MOSFET parasitic capacitance assumption, by substitute Equation (5) into Equations (3) and (4), we can obtain that

$$I_D = \begin{cases} 0, x < \dfrac{\varepsilon_0 V_T}{\sigma} \\ K_N\left[2\left(\dfrac{\sigma x}{\varepsilon_0} - V_T\right)V_{DS} - V_{DS}^2\right], \dfrac{\varepsilon_0 V_T}{\sigma} < x < \dfrac{\varepsilon_0 V_{Dsat}}{\sigma} \\ K_N\left(\dfrac{\sigma x}{\varepsilon_0} - V_T\right)^2, x > \dfrac{\varepsilon_0 V_{Dsat}}{\sigma} \end{cases} \quad (6)$$

Table 1. Parameters for TENGs used in calculation.

TENG	Mode	Σ	S	d_0	g
AC1 (2.1.1, 2.2.1)	Attached-electrode contact	100 nC m^{-2}	N/A	N/A	N/A
FC1 (2.1.2)	Free-standing contact	100 nC m^{-2}	4 mm^2	25 μm	200 μm
FC2 (2.2.2)			12 mm^2		
AC2 (2.1.3, 2.2.3)	Attached-electrode contact	100 μC m^{-2}	1 cm^2	50 μm	N/A

We have used the TENG with parameters as AC1 shown in **Table 1** and n-type MOSFET (NMOS) model described in **Table 2**. Using these parameters and Equations (5)–(7), the $I_D - V_{DD}$ curve of MOSFET under different TENG output is shown in Figure S1b (Supporting Information).

With the basic relationship between TENG output and MOSFET response, motion-controlled logic operations can be realized. Inverter is the basic building block in digital electronics. One of the simplest forms of inverter is constructed using a single NMOS/p-channel MOSFET (PMOS) transistor loaded with a resistor. The TENG can act as the inverter input to realize a mechanical–electronic interface. A TENG-powered NMOS inverter is shown in **Figure 1**a. The TENG is used as input for gate electrode, the source electrode of MOSFET was grounded, a resistor R_D was connected in series with the NMOS on the drain electrode on one side, and connected to a DC voltage V_{DD} on the other side. The output voltage of the NMOS inverter V_{OUT} equals to V_{DS} of the NMOS. Depending on the working status of the TENG, the performance of this NMOS inverter can vary.

Now we analyze the output of the inverter V_{OUT}. From Kirchhoff's Law, we have the relationship

$$V_{OUT} = V_{DD} - I_D R_D \quad (7)$$

Thus, as for the relationship between the displacement of the TENG and V_{OUT} of the inverter, there are also three regions.

(1) When $V_{GS} < V_T$, NMOS is working at the off region ($I_D = 0$), and the inverter is "ON," V_{OUT} is logic "1." For x we have $x < V_T\varepsilon_0/\sigma$

$$V_{OUT} = V_{DD} \quad (8)$$

(2) When $V_{GS} > V_T$, $V_{OUT} > V_{GS} - V_T$, the load line of the resistor will first coincide with the NMOS in its saturation region.

$$\frac{V_T\varepsilon_0}{\sigma} < x < \frac{\varepsilon_0}{\sigma}\left(V_T + \frac{1 - \sqrt{1 - 4K_N R_D K_N V_{DD}}}{2K_N R_D}\right)$$

Table 2. Parameters for MOSFETS used in numerical calculation.

	V_T [V]	K_N/K_P [Ω^{-1}]
NMOS	0.43	1.15×10^{-4}
PMOS	0.4	3.0×10^{-5}

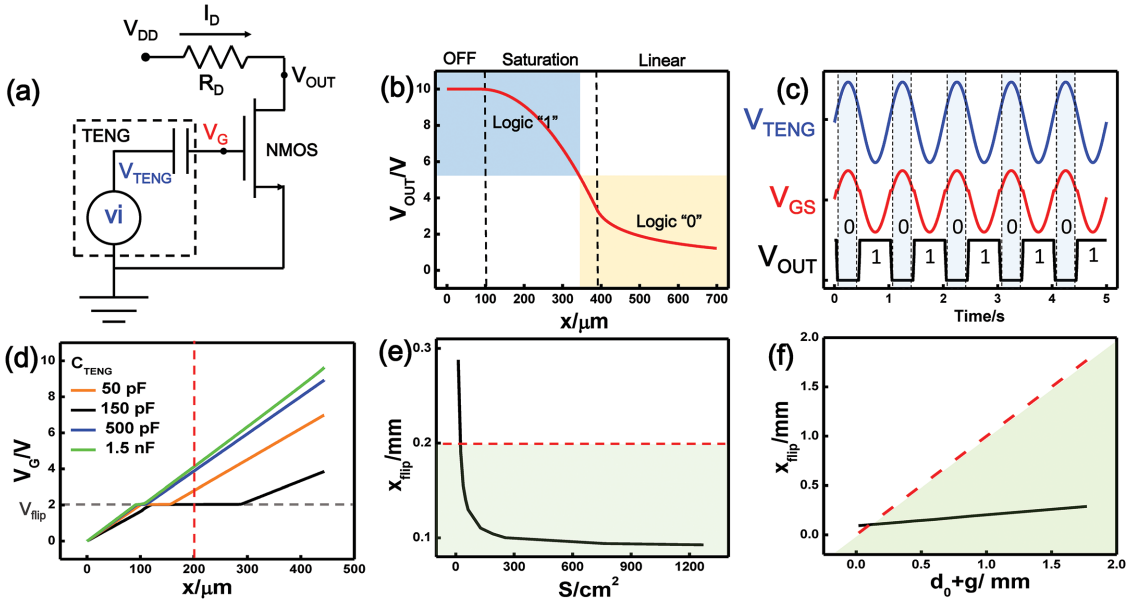

Figure 1. NMOS inverter gated by fixed capacitance TENG. a) Circuit scheme of tribotronic device using TENG as circuit input for a NMOS inverter. b) Calculated behavior of the NMOS inverter (parameters from Table 2) gated by TENG (parameters AC1 from Table 1) neglecting the parasitic capacitance of NMOS. As the displacement of TENG x goes up, the logic output of the inverter goes from "1" to "0." c) The value of V_{TENG}, V_{GS}, and V_{OUT} over 5 s for an NMOS inverter gated by free-standing contact-mode TENG. The NMOS used in the simulation is 2N7000 and TENG is FC1 from Table 1. d) The relationship between V_{GS} and x when σ stays 100 nC m^{-2} and C_{TENG} changes. The red dashed line is $x = g = 200$ μm. e) The relationship between x_{flip} and S when σ, d_0, and g stay the same. The red dashed line is $x = g = 200$ μm. f) The relationship between x_{flip} and $d_0 + g$ when σ and S stay the same. The red dashed line is $x = g$ and the shadowed area is where the inversion can be realized.

$$V_{OUT} = V_{DD} - R_D K_N \left(\frac{\sigma x}{\varepsilon_0} - V_T \right)^2 \tag{9}$$

(3) When V_{GS} exceeds the saturation point, the load line of the resistor will coincide with the NMOS in its linear region, and inverter is off "OFF," V_{OUT} goes to logic "0"

$$x > \frac{\varepsilon_0}{\sigma} \left(V_T + \frac{1 - \sqrt{1 - 4K_N R_D K_N V_{DD}}}{2K_N R_D} \right)$$

$$V_{OUT} = \frac{1}{2R_D K_N} + \frac{\sigma x}{\varepsilon_0} - V_T - \frac{1}{R_D} \sqrt{\left(\frac{\sigma x}{\varepsilon_0} - V_T \right)^2 R_D^2 + \frac{1}{4K_N^2} + \frac{R_D}{2K_N} \left(\frac{\sigma x}{\varepsilon_0} - V_T - V_{DD} \right)} \tag{10}$$

We take the typical value R_D = 1000 Ω, V_{DD} = 10 V, parameters for TENG is the same as in Table 1 and parameters for NMOS is shown in Table 2. By substituting these parameters into Equations (7)–(12), the calculation result is shown in Figure 1b, and we can see that the inversion is successfully realized, and as x increase from 0 to about 1 mm, the output is logically expressed as "1" to "0." With this characteristic, this device can easily be integrated into more sophisticated circuit.

2.1.2. NMOS Inverter Gated by TENG with Constant Capacitance

The first-order equivalent circuit of a TENG contains an AC power source in series with a capacitor, as shown in Figure 1a. And in real applications, the inherent TENG capacitance is in the same order of magnitude compared with parasitic capacitance of MOSFET, leading to a large portion of TENG voltage distributed on the inherent TENG capacitance. Therefore, the coupled MOSFET gate voltage V_{GS} is much smaller than the TENG open-circuit voltage V_{TENG}. Leakage current will be induced in the AC mode through the capacitance and the current equation can be listed as

$$\frac{V_{DD} - V_{OUT}}{R_L} = C_{DG} \frac{d(V_{DS} - V_{GS})}{dt} + I_D = C_{TENG} \frac{d(V_{GS} - V_{TENG})}{dt} + C_{GS} \frac{dV_{GS}}{dt} \tag{11}$$

First, we consider a simplest case, in which the TENG capacitance is a constant and independent of x. As an example, we consider a free standing contact-mode TENG. In this TENG, its open-circuit voltage and inherent capacitance can be given by[16]

$$V_{TENG} = \frac{2\sigma x}{\varepsilon_0} \tag{12}$$

$$C_{TENG} = \frac{\varepsilon_0 S}{d_0 + g} \tag{13}$$

In the above equation, the effective dielectric thickness d_0 is defined as the summation of all the thicknesses of the dielectric d_i between the two metal electrodes divided by its relative effective permittivity ε_{ri}, and g is the gap size between the electrodes.

From Equation (13), we can see that the inherent capacitance C_{TENG} is independent of x, and thus independent of V_{TENG}.

Therefore, the coupled gate voltage can be given by

$$V_{GS} = \frac{V_{OUT}C_{DG} + 2\dfrac{\sigma x S}{d_0 + g} + Q_D}{C_{DG} + \dfrac{\varepsilon_0 S}{d_0 + g} + C_{GS}} \tag{14}$$

where Q_D is the integral of I_D over time, which equals to the accumulative amount of charge going through the drain electrode. Considering the MOSFET work region, Equation (14) can be solved analytically by substituting the value of V_{OUT} from Equations (8)–(10).

$$V_{GS} = \begin{cases} \dfrac{V_{DD}C_{DG} + 2\dfrac{\sigma x S}{d_0 + g}}{C_{DG} + \dfrac{\varepsilon_0 S}{d_0 + g} + C_{GS}}, \text{ inverter ON} \\ \dfrac{V_{var}(x)C_{DG} + 2\dfrac{\sigma x S}{d_0 + g} + Q_{Dsat}(x)}{C_{DG} + \dfrac{\varepsilon_0 S}{d_0 + g} + C_{GS}}, \text{ inverter saturation} \\ \dfrac{2\dfrac{\sigma x S}{d_0 + g} + Q_{Doff}}{C_{DG} + \dfrac{\varepsilon_0 S}{d_0 + g} + C_{GS}}, \text{ inverter off} \end{cases} \tag{15}$$

where $V_{var}(x)$ is a simplified term varying with x. Thus, from Equation (15), V_{GS} and x will have a linear relationship in the "off" region and "on" region, and a nonlinear relationship in the saturation region.

From the analytical equations, we can also see that the design parameters of TENG including σ, S, d_0, and g have influence on the logical operation of the tribotronics device. For optimized performance of the tribotronics device, these design parameters of TENG should match with the MOSFET used. To get an intuitive sense, a simulation methodology has been designed and numerical simulation has been done.[22,23]

We first calculate a freestanding TENG FC1 shown in Table 1. For this device, C_{TENG} is close to 150 pF. In the simulated circuit, a commercially available NMOS model 2N7000 is chosen, as it has relatively low C_{DG} and C_{GS}, and relationships among V_{TENG}, V_{GS}, and V_{DS} are studied carefully. First, the V_{TENG} is set as a harmonic AC output with frequency of 1 Hz and amplitude of 10 V, as we assume that x of TENG also follows harmonic vibration; C_{TENG} is set as 150 pF in this simulation. Figure 1c shows the response of V_{TENG}, V_{GS}, and V_{OUT} in a time span of 5 s and the inversion is successfully realized in each cycle of 1 s. When the inverter output is logic "1," the value of V_{GS} is close to the value of V_{TENG}; and when the inverter output is logic "0," V_{GS} becomes substantially lower than V_{TENG}. The reason for this observation is that when the NMOS is working in the saturation region, the voltage drop on C_{TENG} $V_{drop} = V_{TENG} - V_{GS}$ is larger than V_{drop} when NMOS is working in "off" region or linear region, referring to Equation (11), I_D is the largest in the saturation region, and voltage drop $V_{TENG} - V_{GS}$ is the largest.

For a better understanding, for a MOSFET inverter, if its threshold gate voltage for inversion is a fixed value V_M, from Equation (15) we have

$$x_{flip} = \frac{V_M(\varepsilon_0 S + (C_{DG} + C_{GS})(d_0 + g)) - Q_{Doff}}{2\sigma S} \tag{16}$$

How V_{GS} changes with x under different values of C_{TENG} is plotted in Figure 1d. Here we can see there are three regions in the $V_{GS} - x$ relationship referring to the three regions predicted in Equation (15): as x starts from 0, there is first a linear region where the inverter is "on," and the slope of this region is $2\sigma S/\left[(C_{DG} + C_{GS})(d_0 + g) + \varepsilon_0 S\right]$, and the intersect of this region is $V_{DD}C_{DG}(d_0 + g)/\left[(C_{DG} + C_{GS})(d_0 + g) + \varepsilon_0 S\right]$; followed by a flat "plateau" in Figure 1d where V_{GS} stays at the same value when x increases, where the NMOS is in the saturation region and the inverter is in the transition region from "on" to "off"; and finally another linear region, where the inverter is "off," and the slope of this region is still $2\sigma S/\left[(C_{DG} + C_{GS})(d_0 + g) + \varepsilon_0 S\right]$, and the intersect of this region is 0. We notice that the values of V_{GS} in the "plateau" area are the same for different C_{TENG} values, and smaller C_{TENG} will result in a longer "plateau" and thus larger voltage drop in the saturation region. When the "plateau" is passed in the V_{GS}–x relationship, the output of the inverter will be flipped from "1" to "0" and inversion is completed, and the corresponding V_{TENG} is denoted as V_{flip}. Only when V_{TENG} goes above V_{flip} can the logic operation be realized. Thus, the value of x corresponding to V_{flip}, $x_{flip} = V_{flip}\varepsilon_0/2\sigma$ plays an important role in the device design. For a free-standing contact-mode TENG, the maximized moving distance x can only reach g, so only when x_{flip} is under the limit can the tribotronic device can perform the logic operation.

From Equation (12), the value of σ does not influence the value of C_{TENG}, so the relationship between x_{flip} and $1/\sigma$ is strictly proportional. The relationship between x_{flip} and S, d_0, and g is more complicated, and thus, we can use our simulation methodology to study the influence of S, d_0, and g on the influence of x_{flip} in the same NMOS circuit. For the device operation, the matching of area size S and x_{flip} is important, avoiding the case of either a small device requiring a large displacement to realize the inversion or a large device requiring a tiny displacement. The relationship between x_{flip} and S extracted from the simulated result is shown in Figure 1e. Under a sigma value of 100 nC m^{-2} and value of $d_0 + g$ of 225 μm, the value of x_{flip} descends when the value of S ascends. This trend is also in agreement with the analytical analysis shown in Equation (12), as S is directly proportional to C_{TENG}, and larger C_{TENG} will result in smaller voltage drop on TENG itself, so the coupling of V_{TENG} into the logic circuit will be more efficient. The value of d_0 and g is mainly involved in the fabrication of TENG. Small value of d_0 and g will potentially require more complicated processing and thus higher cost, and will also shorten the mechanical stability and durability of the device. The relationship between x_{flip} and $d_0 + g$ is plotted in Figure 1f, and interestingly, the result is almost linear, consistent with the analytical equation shown above. The operation limit $x = g$ is plotted in Figure 1 d–f as red dashed lines, showing that there

Table 3. MOSFET model used in simulation.

Model no.	Type	C_{DG} [F]	C_{GS} [F]	K_N/K_P [Ω^{-1}]	V_T [V]
2N6659	NMOS	1×10^{-11}	3.2×10^{-7}	0.24	1.72
2N6760	NMOS	1×10^{-11}	7.0×10^{-6}	17.45	3.73
2N7000	NMOS	6×10^{-12}	1.2×10^{-11}	2×10^{-5}	4.73
BST110	PMOS	2.01×10^{-11}	5.71×10^{-11}	1.03×10^{-5}	−2.3
2N6804	PMOS	1×10^{-11}	3.4×10^{-6}	5.22	−3.63

is a minimum value for both S and $d_0 + g$ for TENG fabrication. However, as x value under certain V_{TENG} is proportional to $1/\sigma$, so the limits for S and $d_0 + g$ are extended when σ value increases. Thus, for free-standing contact-mode TENG, whether high value of σ or low value of σ is desired depends on the designed geometric value of S and $d_0 + g$.

We can also study how to choose the right NMOS device for a designed TENG. We have studied three different NMOS, 2N7000, 2N6659, and 2N6760 and their parameters are shown in **Table 3**. Figure S2a (Supporting Information) plots the value of x_{flip} corresponding to different C_{TENG} values for these three NMOS's. From Figure S2a (Supporting Information), we can clearly see that the $x_{flip} - C_{TENG}$ for all three NMOS's show clear reciprocal relationships, which means x_{flip} is proportional to $1/C_{TENG}$, and value of x_{flip} under the same C_{TENG} increases when the parasitic capacitance of NMOS increases. With the plotted Figure for $x_{flip} - C_{TENG}$ for different NMOS's, the match for device design can be easily realized using our simulation methodology.

2.1.3. NMOS Gated by TENG with Variable Capacitance

Most of the TENG designs have inherent capacitance that is variable with x, which means that C_{TENG} depends on x, and the tribotronic device using such a TENG will have different criteria in design. One simple example is an attached electrode contact mode TENG, the capacitance changes with the displacement x. The relationship between x and C_{TENG} is

$$C_{TENG} = \frac{\varepsilon_0 S}{d_0 + x} = \frac{\varepsilon_0 S\sigma}{d_0\sigma + \varepsilon_0 V_{TENG}} \tag{17}$$

From Equation (19), we can clearly see that for this TENG device, C_{TENG} decreases with x and thus decreases with V_{TENG}. For the logic inversion from "1" to "0," the corresponding C_{flip} and x_{flip} will have a relationship

$$x_{flip} = \frac{\varepsilon_0 S}{C_{flip}} - d_0 \tag{18}$$

One easy way to obtain the x_{flip} value for such a device is by solving Equation (18) in series with the $x_{flip} - C_{TENG}$ relationship extracted in Figure S2a (Supporting Information), the coinciding point will show the C_{flip} and x_{flip} values for the TENG device in certain NMOS inverter logic circuit. While for free standing mode TENG, the inversion is limited by the fact that x cannot exceed g, for attached electrode TENG the inversion may also not happen if S or σ is too small or d_0 is too large, as C_{TENG} will always decrease when x increases, and there may be no coinciding point for Equation (18) and the $x_{flip} - C_{TENG}$ equation. Thus, the design is more restricted than in the free-standing contact mode TENG.

For a more thorough study, we substitute Equation (19) into Equation (11)

$$V_{GS} = \frac{V_{DS}C_{DG} + \dfrac{\sigma x S}{d_0 + x} + Q_D}{C_{DG} + \dfrac{\varepsilon_0 S}{d_0 + x} + C_{GS}} \tag{19}$$

From Equation (19), the relationship between V_{GS} and x will be much more complicated than linear. As C_{TENG} decreases when x increases, to ensure the logic inversion can be realized, V_{TENG} should be efficiently coupled into the logic circuit, so C_{TENG} should be kept at a higher value so $V_{TENG} = V_{flip}$ can be reached, and both high values of S and σ are required for such device. As d_0 determines the maximum value of C_{TENG} and the value of C_{TENG} when x is small, and smaller d_0 will effectively lower the value of V_{flip}.

We have used simulation method to study the influence of S, σ, and d_0 on the logic operation and to prove our analytical analysis. **Figure 2**a shows the response of V_{TENG}, V_{GS}, and V_{OUT} in a time span of 5 s, for an attached electrode contact mode TENG device AC2 with size of 1 cm × 1 cm, σ of 100 μC m^{-2}, and d_0 of 50 μm. We can see that the inversion from "1" to "0" is successfully realized in each cycle. However, when $0 < x < x_{flip}$, the NMOS is always in the saturation region and V_{GS} is always in the "plateau" value. Using our simulation method, we have plotted in Figure 2b–d the V_{GS}–x relationship under different S, σ, and d_0 values that can be realized in existing TENG designs. From these results, it is shown that larger S and larger σ will effectively reduce the x_{flip} required for logic inversion, and low values of S and σ will result in the failure of inversion even when x goes to an extremely high value. NMOS is still operating in the saturation region when $x = 0$. When d_0 goes down, the required logic inversion is also reduced. When d_0 goes below 10 μm, then NMOS is in the "on" region when $x = 0$. Depending on the application of such a tribotronics device, the design can be carried out according to our simulation result.

2.2. CMOS Gated by TENG

2.2.1. CMOS Circuit Basics

Compared with inverters composed of a single NMOS or PMOS, CMOS inverter is most commonly used in industry. In a CMOS inverter, the series resistance is replaced by a PMOS, so that there is no static current other than system leakage under either "on" or "off" condition. Besides, the "off" state voltage can effectively reduce to 0. A CMOS inverter gated by the TENG is shown in Figure S1c (Supporting Information), TENG output is connected to the gates of both the PMOS and the NMOS, drain electrode of NMOS

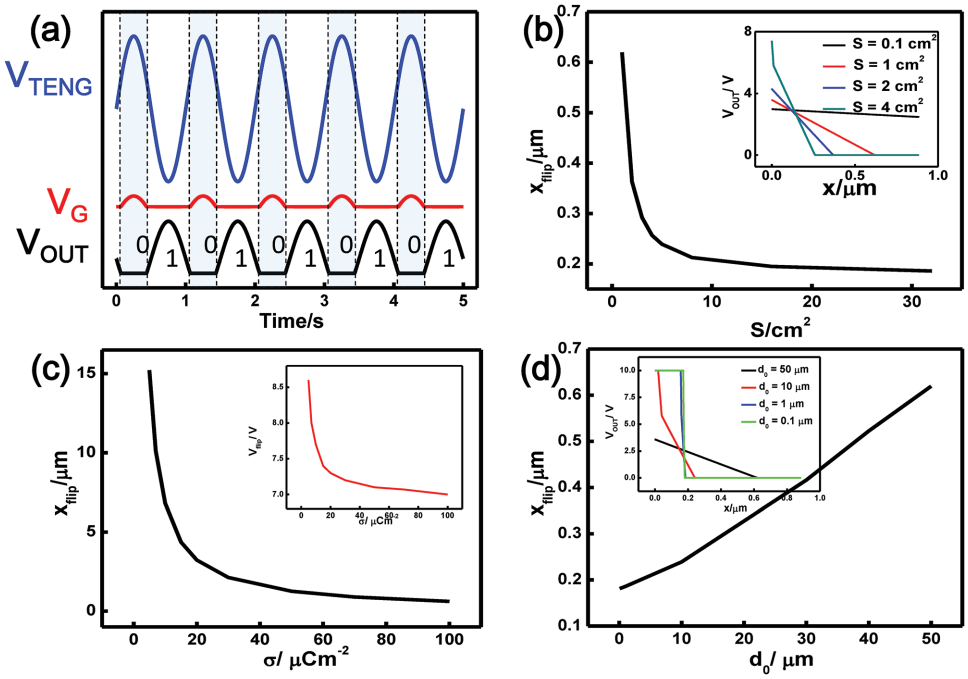

Figure 2. NMOS inverter gated by variable capacitance TENG. a) The value of V_{TENG}, V_{GS}, and V_{OUT} over 5 s for an NMOS inverter gated by attached electrode contact-mode TENG. The NMOS used in the simulation is 2N7000 and TENG is AC1 from Table 1. b) The relationship between x_{flip} and S when σ and d_0 stay the same. Inset is the relationship between V_{OUT} and x under different S values. c) The relationship between x_{flip} and σ when S and d_0 remain the same. Inset is the relationship between V_{flip} and σ when S and d_0 remain the same. d) The relationship between x_{flip} and d_0 when S and σ remain the same. Inset is the relationship between V_{OUT} and x under different d_0 values.

and PMOS are connected together, source electrode of PMOS is connected with a DC power source V_{DD}, and source electrode of NMOS is grounded. From Kirchhoff's law, we have the relationships

$$\begin{cases} I_{DN} = I_{DP} \\ V_{DSN} + V_{SDP} = V_{DD} \\ V_{OUT} = V_{DSN} \\ V_{TENG} = V_{GSN} = V_{DD} - V_{SGP} \end{cases} \quad (20)$$

Similar to NMOS, for a PMOS, there are also three working modes, off mode, linear mode, and saturation mode, and the current equations for these three modes are

$$I_{DP} = \begin{cases} 0; V_{SG} < V_{TP} \\ K_P[2(V_{SG} - V_{TP})V_{SD} - V_{SD}^2]; V_{SG} < V_{TP}, V_{SD} < V_{SG} - V_{TP} \\ K_P(V_{SG} - V_{TP})^2; V_{SG} < V_{TP}, V_{SD} > V_{SG} - V_{TP} \end{cases} \quad (21)$$

A more intuitive graph is shown in Figure S1d (Supporting Information). In this Figure, a NMOS model 2N6659 and a PMOS model 2N6804 is chosen, V_{DD} is set as 10 V, thus I_{DN} $-V_{DSN}$ and I_{DP} $-$ (V_{DD} $-V_{SDP}$) curves are plotted on the same x and y axis. For a specific V_{GS} value, I_{DN} and I_{DP} will coincide a specific value of V_{DSN}, and by plotting each V_{GS} value with the corresponding coincided V_{DSN} value, we have retrieved the relationship between V_{IN} (V_{GS}) and V_{OUT} (V_{DSN}) of the CMOS inverter.

When TENG is working at quasi-steady state, as the output increases from 0 to above V_{Gmax}, the output of CMOS inverter changes gradually. By analytically solving Equation (20), we find that depending on the working mode of NMOS and PMOS, there are five working regions for the CMOS inverter.

(1) NMOS is working at off mode, and PMOS is working at linear mode. $x < \dfrac{V_{TN}\varepsilon_0}{\sigma}$

$$V_{OUT} = V_{DD} \quad (22)$$

(2) NMOS in saturated mode, PMOS in linear mode,

$$\frac{V_{TN}\varepsilon_0}{\sigma} < x < \frac{\left(\sqrt{\frac{K_P}{K_N}}(V_{DD} - V_{TP}) + V_{TN}\right)\varepsilon_0}{\left(1 + \sqrt{\frac{K_P}{K_N}}\right)\sigma}$$

$$V_{OUT} = \frac{\sigma x}{\varepsilon_0} - V_{TP} + \sqrt{\left(V_{DD} - \frac{\sigma x}{\varepsilon_0} - V_{TP}\right)^2 - \frac{K_N}{K_P}\left(\frac{\sigma x}{\varepsilon_0} - V_{TN}\right)^2} \quad (23)$$

(3) NMOS and PMOS are both in saturated mode,

$$x = \frac{\left(\sqrt{\frac{K_P}{K_N}}(V_{DD} - V_{TP}) + V_{TN}\right)\varepsilon_0}{\left(1 + \sqrt{\frac{K_P}{K_N}}\right)\sigma}$$

$$\frac{\sigma x}{\varepsilon_0} - V_{TN} + \sqrt{\left(\frac{\sigma x}{\varepsilon_0} - V_{TN}\right)^2 - \frac{K_P}{K_N}\left(V_{DD} - \frac{\sigma x}{\varepsilon_0} - V_{TP}\right)^2} < V_{OUT} < \frac{\sigma x}{\varepsilon_0} + V_{TP} + \sqrt{\left(V_{DD} - \frac{\sigma x}{\varepsilon_0} - V_{TP}\right)^2 - \frac{K_N}{K_P}\left(\frac{\sigma x}{\varepsilon_0} - V_{TN}\right)^2} \quad (24)$$

which means that when x passes this point, a steep decrease in V_{OUT} will occur, so inversion with the CMOS inverter is more effective than the NMOS inverter.

(4) NMOS in linear mode, and PMOS in saturated mode,

$$\frac{\left(\sqrt{\frac{K_P}{K_N}}(V_{DD} - V_{TP}) + V_{TN}\right)\varepsilon_0}{\left(1 + \sqrt{\frac{K_P}{K_N}}\right)\sigma} < x < \frac{(V_{DD} - V_{TP})\varepsilon_0}{\sigma}$$

$$V_{OUT} = \frac{\sigma x}{\varepsilon_0} - V_{TN} + \sqrt{\left(\frac{\sigma x}{\varepsilon_0} - V_{TN}\right)^2 - \frac{K_P}{K_N}\left(V_{DD} - \frac{\sigma x}{\varepsilon_0} - V_{TP}\right)^2} \quad (25)$$

(5) NMOS is working at off mode, and PMOS is working at linear mode, $x > \frac{(V_{DD} - V_{TP})\varepsilon_0}{\sigma}$

$$V_{OUT} = 0 \quad (26)$$

Figure 3b shows the inversion performance of an inverter using Equations (22)–(26). The parameters for TENG is AC1 in Table 1, NMOS and PMOS parameters are the same as in Table 2. The range of x for CMOS inversion is similar to the range of x in NMOS inversion in Figure 1d. The steep inversion at the point when NMOS and PMOS are both at the saturation region is observed when x = 312 μm. The calculation shows that TENG can power CMOS inverter as good as NMOS, and on the basis of current experimental results, CMOS inversion can be easily realized without complicated modification for the devices.

2.2.2. CMOS Gated by TENG with Constant Capacitance

When TENG is working at AC mode, similar to NMOS inverter, we have

$$\frac{V_{DD} - V_{OUT}}{R_L} = C_{DGP}\frac{d(V_{DS} - V_{GS})}{dt} + I_D = C_{TENG}\frac{d(V_{GS} - V_{TENG})}{dt} + C_{GSN}\frac{dV_{GS}}{dt} \quad (27)$$

The solution of Equation (27) with a free standing contact mode TENG gives

$$V_G = \frac{V_{OUT}C_{GDP} + 2\frac{\sigma x S}{d_0 + g} + Q_D}{C_{GDP} + \frac{\varepsilon_0 S}{d_0 + g} + C_{GSN}} \quad (28)$$

By substituting Equations (22)–(26) into Equation (28), we can see there are five phases in the $V_{TENG} - V_{GS} - V_{OUT}$ relationship. Before the inversion from logic output of "1" to "0" is completed, there will be three transition phases where either or both NMOS and PMOS are in saturation region.

Again, we use simulation method to study such a tribotronic device. Figure 3c shows the calculation result of how TENG can drive the CMOS inverter and realize the inversion of signals. In this simulation, the TENG is working at frequency of 1 Hz amplitude of 20 V, and C_{TENG} is set as 150 pF. NMOS is chosen as 2N7000 and PMOS is chosen as BST110 as these two MOSFETs have low parasitic capacitance, as shown in Table 2. The inversion from "1" to "0" is successfully realized when TENG operates and

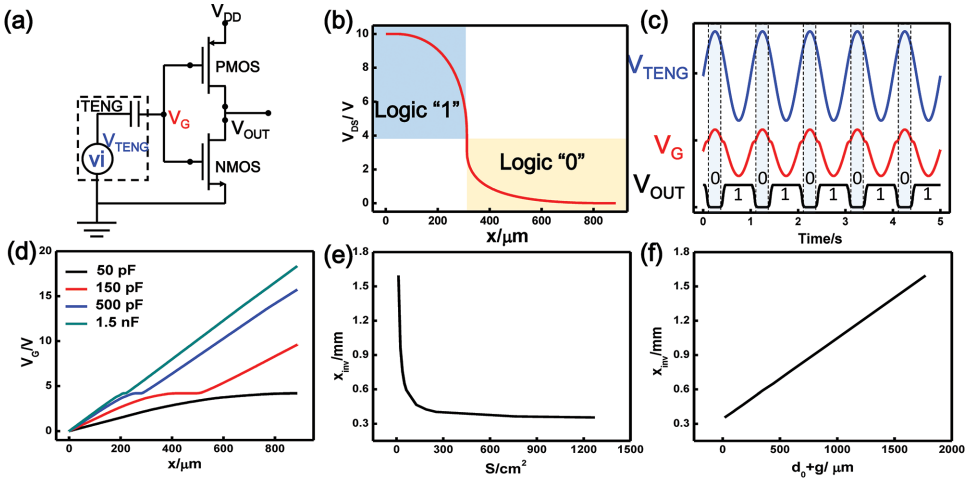

Figure 3. CMOS inverter gated by fixed capacitance TENG. a) Circuit scheme of tribotronic device using TENG as circuit input for a CMOS inverter. b) Calculated behavior of the CMOS inverter (parameters from Table 2) gated by TENG (parameters AC1 from Table 1) neglecting the parasitic capacitance of CMOS. As the displacement of TENG x goes up, the logic output of the inverter goes from "1" to "0." c) The value of V_{TENG}, V_{GS}, and V_{OUT} over 5 s for a CMOS inverter gated by free-standing contact-mode TENG. The NMOS used in the simulation is 2N7000, PMOS is BST110, and TENG is FC2 from Table 1. d) The relationship between V_{GS} and x when σ stays 100 nC m^{-2} and C_{TENG} changes. e) The relationship between x_{flip} and S when σ, d_0, and g stay the same. f) The relationship between x_{flip} and $d_0 + g$ when σ and S stay the same.

x changes from 0 to 883 μm. However, the transition from "1" to "0" is slower than in the NMOS inverter, which comes from the transition phases mentioned in the analytical part. By plotting the $V_{GS} - x$ relationship under different C_{TENG}, the five phases according to our analytical result shows clearly: as x starts from 0, there is first a linear $V_{GS} - x$ relationship referring to the "on" mode for the CMOS output; a nonlinear region follows referring to the saturation mode of NMOS and linear mode of PMOS; a flat "plateau" similar to the "plateau" in NMOS referring to the saturation mode of both NMOS and PMOS; another nonlinear region referring to the linear mode of NMOS and saturation mode of PMOS; and following is a linear region referring to the "off" mode of CMOS output where the inversion is completed. Thus, the completion of the inversion is characterized by the value of x when $V_{GS} - x$ relationship enters the last region, and we call this value x_{inv}. In Figure 3e,f, we have accordingly plotted the relationship of $x_{inv} - S$, and $x_{inv} - d_0 + g$. The result shows again that x_{inv} is proportional to $1/S$, and a linear relationship between x_{inv} and $d_0 + g$, meaning that the value of V_{GS} required to realize the inversion is independent of the inherent capacitance of the TENG.

2.2.3. CMOS Gated by TENG with Capacitance Changing by Output

The solution of Equation (29) with an attached-electrode contact mode TENG gives

$$V_G = \frac{V_{DSN} C_{GDP} + \frac{\sigma x S}{d_0 + x} + Q_D}{C_{GDP} + \frac{\varepsilon_0 S}{d_0 + x} + C_{GSN}} \tag{29}$$

Using the same simulation method as in Section 2.1.2 and the same device setup as in Section 2.2.1, the simulation on tribotronics device based on attached electrode contact mode TENG is shown in Figure S3 (Supporting Information). Figure S3a (Supporting Information) shows the inversion behavior of such a TENG in 5 s and Figure S3b–d (Supporting Information) shows the relationship between x_{inv} and the design parameters of TENG, S, sigma, and d_0. The result not only gives instruction for design of TENG but also confirms that the logic operation of the inverter only depends on the V_{GS} applied onto the gate electrode, and thus the inherent capacitance of the TENG only influences the coupling efficiency from output of TENG into the input of the logic device.

2.3. Examples of Logic Operations

With our methodology, we can test the realization of more complicated logic operation using tribotronic device. As a simple demonstration of logic operation, negative-AND (NAND) gate and negative-OR (NOR) gate using two TENGs are simulated. As shown in **Figure 4**a, the NAND circuit is composed of two PMOS connected parallel (1 and 2) in series with two NMOS connected in series (3 and 4). Two TENGs (A and B) are used to control the gate voltage of one PMOS and one NMOS each. The logic operation through this circuit is $OUT = \overline{A \cdot B}$. The circuit is simulated using previous method, NMOS is chosen as 2N7000 and PMOS is chosen as BST110. For both TENGs, the output of the TENG is set as pulse output to demonstrate the logic operation, the parameters for TENG design is FC1 in

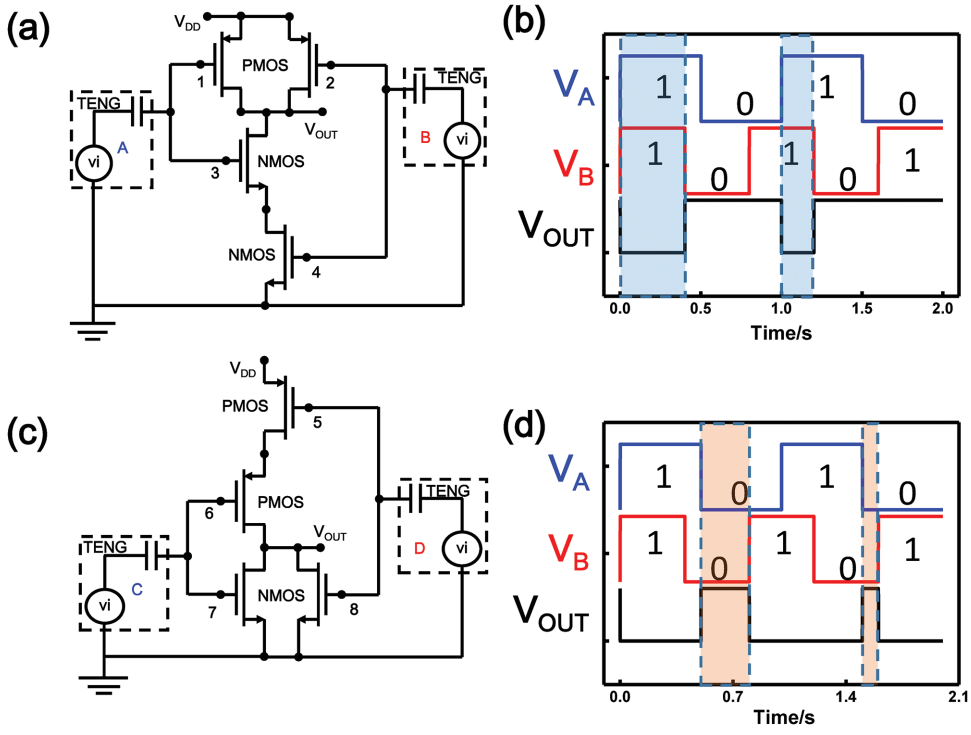

Figure 4. Demonstration of logic operation realized by tribotronics device. a) Circuit scheme of NAND logic gated by TENGs. b) Simulation result of the NAND logic output when input of the TENGs has different values. c) Circuit scheme of NOR logic gated by TENGs. d) Simulation result of the NOR logic output when input of the TENGs has different values.

Table 1, size of TENG is 2 mm × 2 mm so C_{TENG} = 150 pF, σ is set as 100 nC m^{-2} and x is set as 883 mm so V_{TENG} = 20 V. From the simulation result shown in Figure 4b, the logic operation works well: When the A = B = 1, OUT = 0; otherwise, OUT = 1.

As shown in Figure 4c, the NOR circuit is composed of two PMOS connected series (5 and 6) in series with two NMOS connected in parallel (7 and 8). Two TENGs (C and D) are used to control the gate voltage of one PMOS and one NMOS each. The MOSFETs and TENG are set the same as in the NAND circuit. The logic operation through this circuit is $OUT = \overline{C + D}$. From the simulation result shown in Figure 4d, the logic operation works well: when C = D = 0, OUT = 1; otherwise, OUT = 0.

3. Mechanical Sensing of TENG by MOSFET Circuit

Resistor loaded MOSFET transistor is also commonly used as small signal amplifier.[24–27] Under DC bias in V_{IN} of MOS transistor, a small AC signal can be coupled into the input, and as V_{GS} changes, V_{OUT} will change accordingly, so the AC signal will be amplified. Such amplification can be utilized in tribotronic device as an effective mechanical sensor. The circuit for small signal sensing is schemed in **Figure 5**a. In such a circuit, R1 and R2 are utilized to provide a DC bias to the MOSFET. To analyze the gain of such a circuit, the small signal equivalent circuit is shown in Figure 5b. We have carried out analytical analysis for the frequency response when C_{TENG} is added in the circuit, and developed the method to optimize the gain using simulation method.

3.1. NMOS Small Signal Analysis with TENG

From the equivalent circuit illustration of an NMOS amplifier in Figure 5a, using Kirchhoff's law, we have the current equations for each node

$$\frac{V_{TENG} - V_1}{\frac{1}{j\omega C_{TENG}}} = \frac{V_1}{\frac{1}{j\omega C_{GS}}} + \frac{V_1 - V_2}{\frac{1}{j\omega C_{GD}}} \tag{30}$$

$$\frac{V_1 - V_2}{\frac{1}{j\omega C_{GD}}} = g_m V_1 + \frac{V_2}{R_L} \tag{31}$$

where g_m is the intrinsic transconductance of the MOSFET $g_m = \partial I_{DS}/\partial V_{GS}$, which is an important figure of merit showing how the drain current respond to change of gate voltage.

By solving Equations (30) and (31), we have

$$V_1 = V_{TENG} \frac{C_{TENG}}{C_{TENG} + C_{GS} + C_{GD} \frac{g_m R_L + 1}{j\omega C_{GD} R_L + 1}} \tag{32}$$

$$V_2 = V_{TENG} \frac{C_{TENG}(j\omega C_{GD} R_L - g_m R_L)}{C_{TENG}(j\omega C_{GD} R_L + 1) + C_{GS}(j\omega C_{GD} R_L + 1) + C_{GD}(g_m R_L + 1)} = V_{TENG} A_V \tag{33}$$

The current can be expressed as

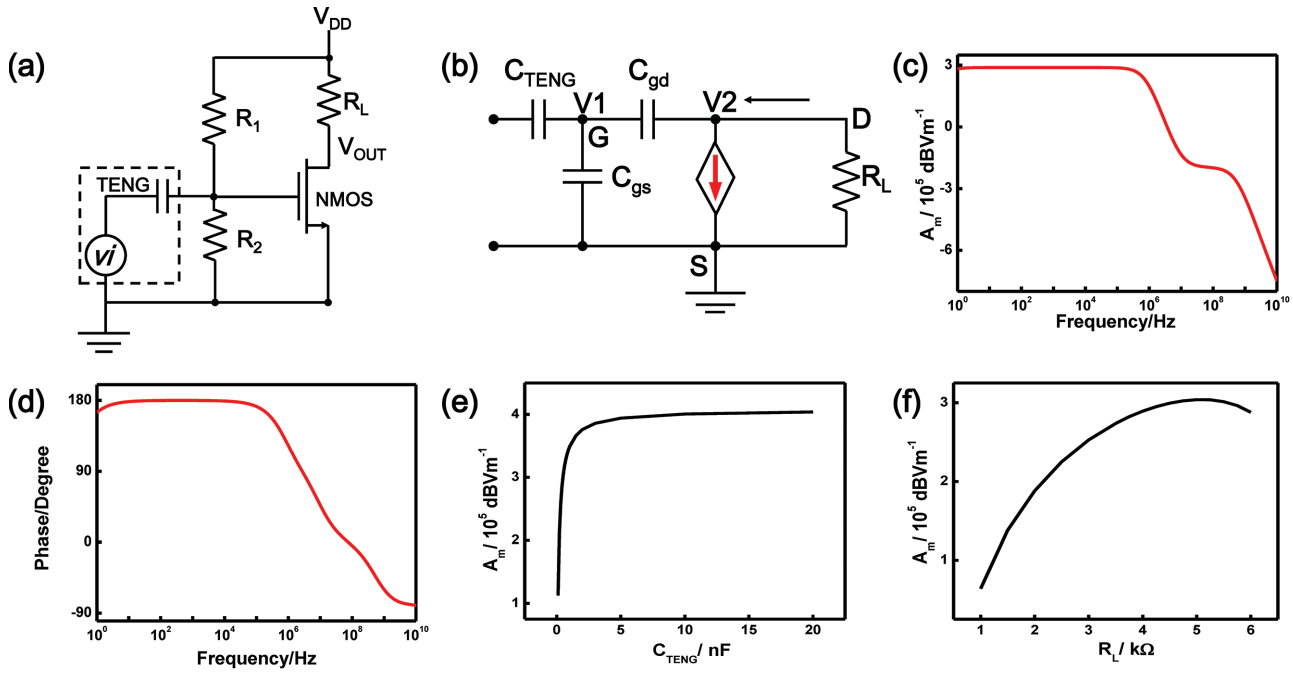

Figure 5. Small signal analysis of tribotronic device. a) Circuit scheme of small signal model of tribotronic device. b) Equivalent circuit of the small signal model shown in Figure 5a. c) Change of small signal gain over frequency range. d) Change of phase over frequency range. e) Relationship between gain and C_{TENG}. f) Relationship between gain and R_L.

$$i = g_m V_1 = g_m V_{TENG} \frac{C_{TENG}}{C_{TENG} + C_{GS} + C_{GD}\frac{g_m R_L + 1}{j\omega C_{GD} R_L + 1}} \quad (34)$$

And the effective transconductance counting TENG is

$$g_{mT} = \frac{\partial I_{DS}}{\partial V_{TENG}} = g_m \frac{C_{TENG}}{C_{TENG} + C_{GS} + C_{GD}\frac{g_m R_L + 1}{j\omega C_{GD} R_L + 1}} \quad (35)$$

The amplification gain A_V

$$A_V = \sqrt{\frac{C_{TENG}\left(-(\omega C_{gd} R_L)^2 + (g_m R_L)^2\right)}{(C_{TENG} + C_{GS} + C_{GD}(g_m R_L + 1))^2 - (C_{TENG} + C_{GS})^2 (\omega C_{GD} R_L)^2}} \quad (36)$$

When frequency is low, the maximum voltage gain for the amplifier

$$A_{Vmax} = \frac{C_{TENG} g_m R_L}{C_{TENG} + C_{GS} + C_{GD}(g_m R_L + 1)} \quad (37)$$

When transconductance is large enough, A_{Vmax} decomposes to

$$A_{Vmax} = \frac{C_{TENG}}{C_{GD}} \quad (38)$$

Since the small signal application usually works in the saturation mode for the DC bias, the transconductance is defined as

$$g_m = \sqrt{2k'\frac{W}{L} I_D} = \sqrt{2k' K_N \frac{W}{L}}(V_G - V_T) \quad (39)$$

Thus, larger V_{GS} will enhance the value of gm. As larger x leads to larger C_{TENG} and V_{TENG}, it is desired to have a larger output from the TENG. However, larger V_{GS} also leads to larger V_{Dsat}. Thus, it also should be taken into account. In design and fabrication of tribotronics devices, the V_{Dsat} should be taken into account, generally, MOSFETs with higher breakdown voltage and lower V_{Dsat} under certain V_{GS} is desired for small signal tribotronic device.

At band width, $A_V = \frac{1}{\sqrt{2}} A_{Vmax}$, so band width frequency

$$f_L = \frac{g_m}{\sqrt{2} C_{GD}} \quad (40)$$

Thus, the bandwidth is hardly affected by the nature of TENG. Considering the sensitivity of the small signal magnification, the mechanical sensitivity A_m can be defined as

$$A_m = \frac{2\sigma A_V}{\varepsilon_0} \quad (41)$$

Depending on the mode of the TENG, A_m can be calculated from A_V according to the $V - x$ relationship of the TENG.

3.2. Simulation Results

First, we have verified the analytical result with circuit simulation for the circuit shown in Figure 5a.[23] The numerical value of parameters in Figure 5a is set as V_{DD} = 10 V, R_1 = 4 GΩ, and R_2 = 1 GΩ, so the DC bias on gate voltage is 8 V, R_L = 4 kΩ, NMOS is 2N6659, and TENG is set as FC2 in Table 1, so C_{TENG} = 500 pF. By substituting Equation (12) into Equation (41),

$$A_m = A_V \frac{V_{TENG}}{x} \quad (42)$$

Since the small signal analysis only involves mechanical perturbation around the DC point, C_{TENG} can be considered as a fixed value no matter what type of TENG is used here, so the analysis also applies to attached-electrode contact mode TENG as well as other TENGs. As shown in Figure 5c, the small signal response A_m at lower frequency is around 2.71×10^5 dBVm^{-1}, and decreases when frequency goes above 10^5 Hz, together with a phase change as shown in Figure 5d.

As shown in Equation (38), there is a linear relationship between maximum A_m and C_{TENG}. In Figure 5e, we have plotted the simulated relationship between C_{TENG} and the maximum A_m when C_{TENG} changes from 500 pF to 30 nF. When C_{TENG} is small, the linear relationship from the analytical results stands; yet when C_{TENG} increases to above 3 nF, the maximum A_m tends to saturate. From Equation (37), the maximum A_m should increase when R_L increases and saturates when $g_m R_L >> 1$. We have also calculated the relationship between R_L and A_m when other parameters stay the same, and the result is shown in Figure 5f. When R_L < 4.5 kΩ, the analytical result also stands, yet when R_L > 4.5 kΩ, A_m begins to decrease. Such a mismatch from the analytical prediction comes from the fact that DC working point has floated from saturation region to linear region when R_L changes and A_m will decrease dramatically. For our simulated circuit, the small signal response is optimized when R_L is around 4.5 kΩ and when C_{TENG} reaches 5 nF. The relationship between A_m and parameters for the TENG can be easily derived from the relationship in Figure 5e using the relationship between C_{TENG} and these parameters.

4. Conclusions

In summary, we have carried out the first theoretical analysis of tribotronic devices. For the mechanical controlled logic, we have studied the commonly used NMOS inverter and CMOS inverter gated by TENG and discussed the influence of TENG mode and design parameters on the logic operation. Through our analysis, the structural parameters control inherent capacitance and influence the coupling efficiency of the TENG output into the logic circuit gate voltage input. Depending on the geometric requirements in the tribotronic device design, our result can be utilized as instruction for choosing the right TENG and logic device. For mechanical signal sensing, we have studied the small signal amplification of the MOSFET circuit gated with TENG. It is discovered that larger TENG capacitance and

higher surface charge density will lead to higher gain in the same small signal circuit, yet depending on difficulty of TENG fabrication and geometry match of devices, our methodology can be utilized to optimize the device design.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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