Tribotronic Logic Circuits and Basic Operations

*Chi Zhang, Li Min Zhang, Wei Tang, Chang Bao Han, and Zhong Lin Wang**

A logic circuit is an idealized physical unit to implement discrete signals transmission and operation, which is a basic element of the integrated circuit and has a wide range of applications in computer, digital control, communications, and instrumentation.[1,2] With the rapid development of nanotechnology in semiconductor, nanomaterials exhibit tremendous potential in logic devices, such as silicon nanowire,[3,4] carbon nanotube,[5,6] graphene,[7,8] and single-layer MoS_2.[9,10] However, the existing logic devices are almost completely triggered or activated by electric potential applied through a gate.

In 2007, piezotronics was first proposed by coupling piezoelectric polarization and semiconductor properties.[11–16] Due to the noncentral symmetry of Wurtzite and zinc blend structures, such as ZnO, GaN, and InN, a piezoelectric potential (*piezopotential*) is created in the crystal by applying a strain. Such piezopotential serves as a "gate" voltage that can effectively tune/control the charge transport across an interface/junction. The electronics fabricated based on such a mechanism is defined as *piezotronics*. Piezotronic logic nanodevices can convert mechanical stimuli into internal electronic controlling signals and perform mechanical–electrical coupled piezotronic logic operations.[17–19] Recently, the invention of a triboelectric nanogenerator (TENG) has not only provided a new energy technology,[20–29] but also opened up a new research field of tribotronics, which is about the devices fabricated using the electrostatic potential created by triboelectrification as a "gate" voltage to tune/control charge carrier transport in the semiconductor.[30] Tribotronics has more choices of semiconductor material than piezotronics, which is very suitable for the interactive application in conjunction with the current silicon integrated circuits.

Here, we developed a floating contact-electric-field gated tribotronic transistor (CGT), which can use the triboelectric charges created by the contact electrification to modulate transport of charge carriers in the channel. Based on two opposite CGTs, a contact-gated tribotronic logic device (CGL) was developed for converting external mechanical stimuli into logic level signals. By further assembling and integrating CGLs, universal combinational logic circuits such as NOT, AND, OR, NAND, NOR, XOR, and XNOR gates were demonstrated for performing mechanical–electrical coupled tribotronic logic operations. With the direct interaction between the external environment and silicon-based circuits, tribotronic logic circuits have potential applications in human-computer interaction, micro/nano-electromechanical system (MEMS/NEMS), intelligent robots, and internet of things.

Dr. C. Zhang, L. M. Zhang, Dr. W. Tang, Dr. C. B. Han, Prof. Z. L. Wang
Beijing Institute of Nanoenergy and Nanosystems
Chinese Academy of Sciences
Beijing 100083, China
E-mail: zlwang@gatech.edu
Prof. Z. L. Wang
School of Material Science and Engineering
Georgia Institute of Technology
Atlanta, GA 30332, USA

DOI: 10.1002/adma.201501511

The structure of the CGT is composed of an inverted silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor (MOSFET) and a mobile polytetrafluoroethylene (PTFE) layer, as schematically illustrated in **Figure 1**a, which has simpler structure and more practicability than previous tribotronic transistor.[30] In the CGT device, two aluminum pads are deposited on the back of the p-type channel layer with Ohmic contacts, serving as the bottom drain and source electrodes. The conduction channel length and width are 200 and 2 μm, respectively. An aluminum layer is deposited on the surface of the heavily doped silicon substrate with Ohmic contact, serving as the top floating gate electrode without any external electrical connection. The buried silicon dioxide layer of 0.1 μm thick between them is used as the gate oxide. The mobile PTFE layer is assembled next to the floating gate, which can vertically contact with and separate from the floating gate by an external force. The working principle of the CGT is based on the coupling effects of MOSFET and TENG with single-electrode mode, which is schematically shown in Figure 1b. When the external force is applied on the device, the floating gate and PTFE layer fully contact with each other for electrification, leaving net positive charges on the floating gate and net negative charges on the PTFE layer. The produced triboelectric charges with opposite polarities are fully balanced at this moment, leading to no influence on the channel layer. When the external force is released, the PTFE layer is separated from the floating gate in a certain distance. The positive charges on the floating gate can induce an inner charge polarization and form a depletion zone in this p-type channel, which will decrease the channel width and thus the drain current. When the external force is applied and the PTFE layer contacts with the floating gate again, the positive charges on the floating gate are balanced by the negative charges on the PTFE layer and has no effects on the channel layer. The channel width and drain current will be increased and recovered to the original state. Therefore, the CGT can be gated by the external force with the process of contact and separation between the mobile layer and the floating gate, which has the same effect as injecting charges on the floating gate as in conventional transistor.

Figure 1c shows the I_{DS}–V_{DS} characteristics of the CGT with different vertical distances between the PTFE layer and gate electrode from 0 to 1.2 mm, and Figure 1d shows the I_{DS}–d characteristics of the CGT at different drain voltages. The distance is well-controlled and measured by a precise positioning system, which is schematically illustrated in Figure S1, Supporting Information. The experimental results indicate that the drain current is decreased with the increasing vertical distance, which is in accordance with the working principle. At a drain voltage

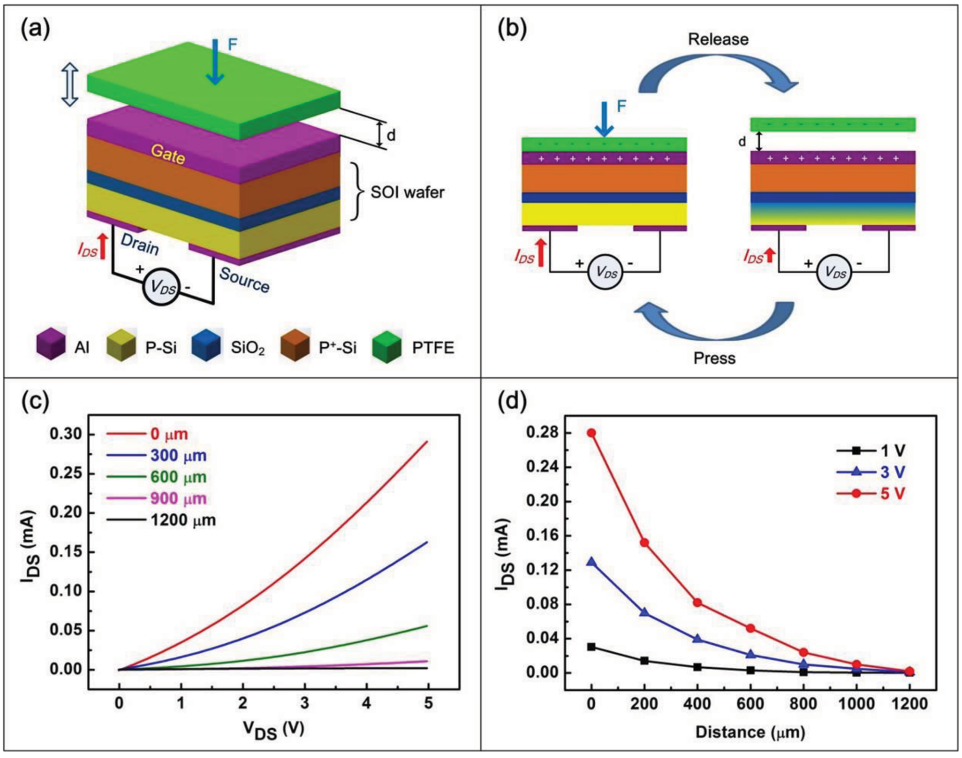

Figure 1. Floating contact-electric-field gated tribotronic transistor (CGT). a) Structure of the CGT based on a MOSFET and a mobile layer for vertical contact electrification. b) Change of the channel width and drain current when the external force is applied and released to demonstrate the working principle. c) I_{DS}–V_{DS} characteristics of the CGT with different vertical distances between the PTFE layer and gate electrode. d) I_{DS}–d characteristics of the CGT at different drain voltages.

of 5 V, the drain current is decreased from 0.28 mA to 2.0 μA in the separation process. It is worth noting that drain current keeps a very rapid decrease when the contacted PTFE layer starts to separate, until the distance is close to about 1.2 mm. At this distance, the positive charges on the floating gate are almost completely away from the screening by the PTFE layer. For the characteristics, it is defined as the on-state for the CGT device when the PTFE layer contacts with the floating gate, while the off-state when the distance is 1.2 mm or above.

The structure of the CGL is schematically illustrated in **Figure 2**a, which is based on two opposite CGTs. In the CGL device, two mobile PTFE layers are supported by the acrylic sheet, which can vertically contact with or separate from the two floating gates, respectively. The vertical moving range D_0 is set as 1.2 mm. The drain of the lower CGT is supplied by the power source of V_{bias} and the source of the upper CGT is connected to ground. The source of the lower CGT is connected to the drain of the upper CGT as the output port of V_{out}. The equivalent circuit of the CGL is shown in Figure 2b, which is composed of two FETs and a TENG. The TENG is driven by the external force and can provide dual-gate voltages for the two FETs, respectively. Figure 2c shows the V_{out}–d transfer characteristic of the CGL at a fixed bias of 5 V, which indicates that the output voltage is decreased with the increasing vertical distance. For the complementary metal-oxide-semiconductor (CMOS) logic level standard, the moving range in $d \leq d_{IL}$ (308 μm) induces an output voltage above point A (4.5 V), which is defined as the high level range (yellow region) and the logic "1" output region for the CGL. While moving range in $d \geq d_{IH}$ (952 μm) induces the output voltage below point B (0.5 V), which is correspondingly defined as the low level range (blue region) and the logic "0" output region for the CGL.

When the external force is fully released and the PTFE layer contacts the upper floating gate ($d = D_0$), the upper CGT is in on-state and the lower CGT is in off-state, which is defined as the logic "0" input state. While when the external force is fully applied and the PTFE layer contacts the lower floating gate ($d = 0$), the upper CGT is in off-state and the lower CGT is in on-state, which is defined as the logic "1" input state. Figure 2d,e shows the output characteristics and experimental truth table of the CGL at "0" and "1" input states and the insets exhibit the corresponding configuration states of the CGL. The output voltage is 0.034 ± 0.020 V in logic "0" input state, and 4.946 ± 0.021 V in logic "1" input state, which are both in the logic "0" and "1" output regions of the CGL, respectively. The V_{on}/V_{off} ratio of 145 demonstrates a good logic performance for the CGL. Therefore, the output voltage can be on-off switched by the external force and the CGL has established the relationship between the mechanical force and CMOS logic electric level, which is represented by a logic symbol as shown in Figure 2f.

As shown in **Figure 3**a, the ports for V_{bias} and ground are exchanged compared with the CGL. Figure 3b shows the measured output voltages at different states of input force and Figure 3c shows the experimental truth table with physical values following each corresponding logic level. The measurement results can meet the characteristics of the logic

Adv. Mater. **2015**,
DOI: 10.1002/adma.201501511

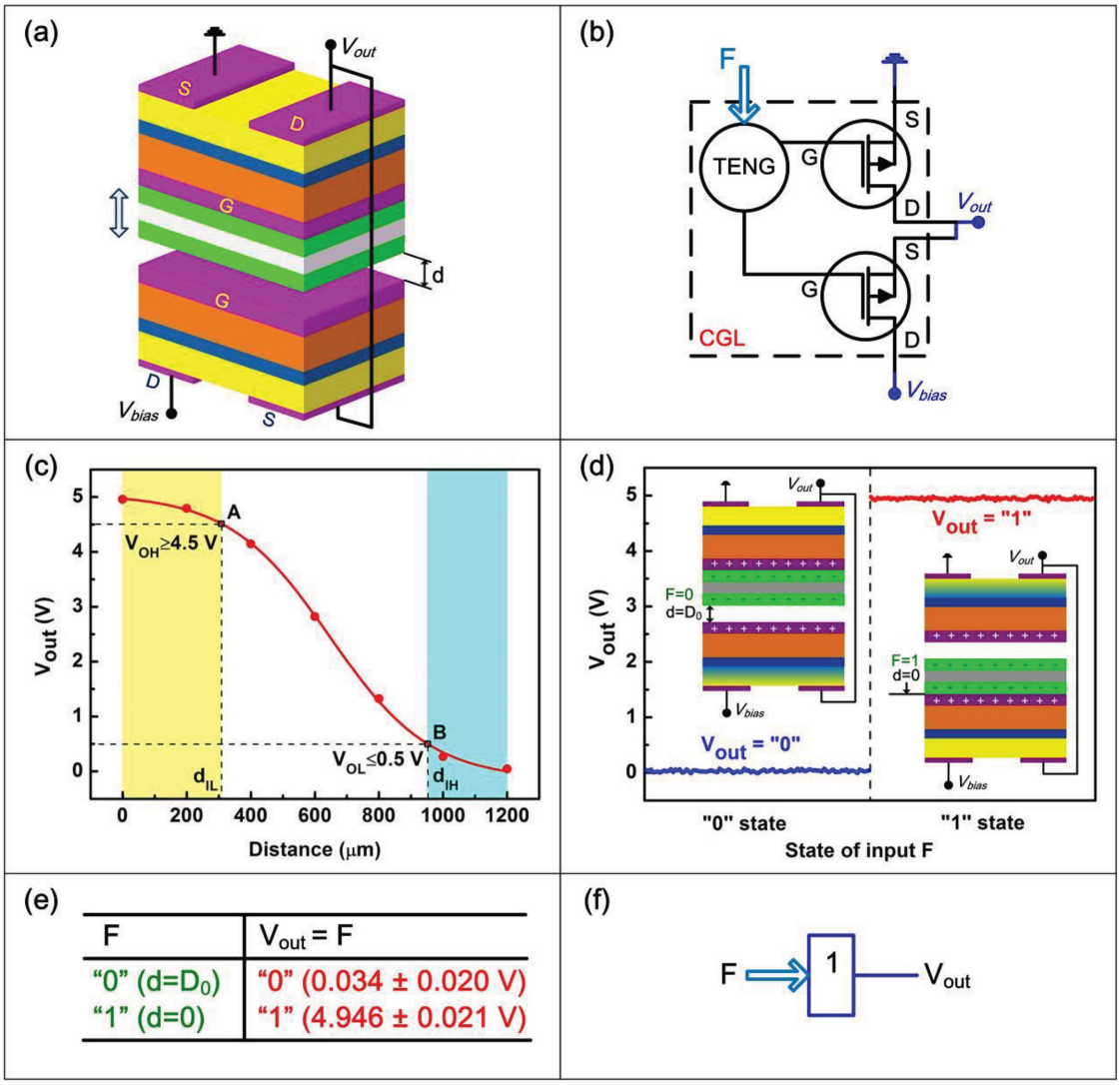

Figure 2. Contact-gated tribotronic logic device (CGL). a) Structure of the CGL based on two opposite CGTs. b) Equivalent circuit of the CGL composed of a TENG and two FETs. c) V_{out}-d transfer characteristic of the CGL at a fixed bias of 5 V. For the CMOS level standard, the output voltage above point A is the high level range (yellow region), which is the logic "1" output region for the CGL. While below point B is the low level range (blue region), which is the logic "0" output region for the CGL. d) Output logic levels at "0" and "1" states of the input force. The insets are the corresponding configuration states of CGL when the external force is fully released ("0" state) and applied ("1" state). e) Experimental truth table of the CGL with physical values following each corresponding logic level. f) Logic symbol of the CGL.

NOT gate and CMOS logic level standard. Therefore, the contact-gated tribotronic logic NOT gate can be correspondingly realized, with a logic symbol as shown in Figure 3d.

Based on two CGLs, the tribotronic AND logic circuit and operation can be realized as shown in **Figure 4**a. In the circuit, the drain of #1 CGT is supplied by the power source of V_{bias} and the source is connected to the drain of #3 CGT. The drains of #2 and #4 CGTs are connected to the source of #3 CGT as the output port of V_{out}, and the sources of #2 and #4 CGTs are connected to the ground. With this connection method, #1 and #3 CGTs are in series and #2 and #4 CGTs are in parallel. The external forces F_A and F_B are applied to the two CGLs, respectively. Figure 4b shows the measured output voltages of the AND gate at different combined states of input F_A and F_B, and Figure 4c shows the experimental truth table with physical values following each corresponding logic level. The measurement results accord well with the characteristics of the logic AND operation and CMOS logic level standard. The logic symbol for the tribotronic AND logic gate is represented in Figure 4d.

As shown in Figure 4e, the drains of #1 and #3 CGTs are supplied by the power source of V_{bias} and the sources are connected to the drain of #4 CGT as the output port of V_{out}. The drain of #2 CGT is connected to the source of #4 CGT and the source of #2 CGT is connected to the ground. With this connection method, #1 and #3 CGTs are in parallel and #2 and #4 CGTs are in series, which is different from and symmetric with the tribotronic AND logic circuit. Figure 4f shows the measured output voltages at different combined states of input F_A and F_B, and Figure 4g shows the experimental truth table with physical

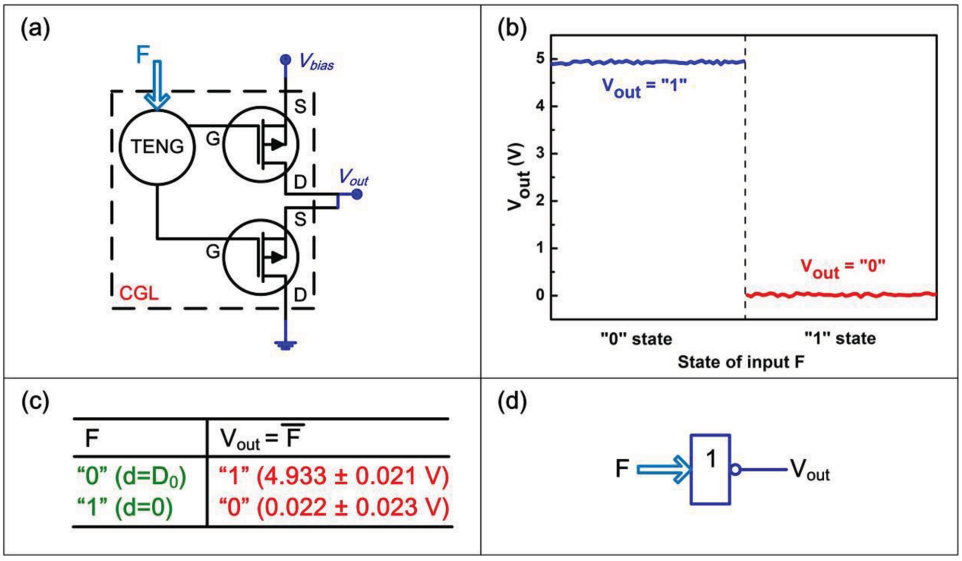

Figure 3. Contact-gated tribotronic logic NOT gate. a) Equivalent circuit of the NOT gate based on the CGL. b) The measured output voltages of the NOT gate at different states of input force. c) Experimental truth table of the NOT gate with physical values following each corresponding logic level. d) Logic symbol of the tribotronic logic NOT gate.

values following each corresponding logic level. The measurement results indicate that the tribotronic logic OR operation is realized with the CMOS logic level standard, which is represented as a logic symbol as shown in Figure 4h.

Similar to the tribotronic AND/OR logic circuits, but with the exchanged ports for V_{bias} and ground, the tribotronic NAND/NOR logic circuits can be realized as shown in **Figure 5**, including the equivalent circuits, output logic levels at different input states, experimental truth tables and logic symbols. The measurement results are logically complementary with the AND/OR logic outputs and have realized the tribotronic NAND/NOR logic operations with the CMOS logic level standard.

The tribotronic XOR/XNOR logic operations need more complicated circuits, which can be configured based on three CGLs as shown in **Figure 6**a,e. In the XOR circuit, the source of #2 CGT and the drain of #3 CGT are supplied by the power source of V_{bias}. The drain of #1 CGT and the source of #4 CGT are connected to the ground. The source of #1 CGT and the drain of #2 CGT are connected to the drain of #5 CGT as the inner signal V_A, while the source of #3 CGT and the drain of #4 CGT are connected to the source of #6 CGT as the inner signal V. The source of #5 CGT is connected to the drain of #6 CGT as the output port of V_{out}. The external force F_A is applied to #1 CGL and #2 CGL simultaneously, and F_B is applied to #3 CGL. For the circuit connection, the #1 CGL is equivalent to a tribotronic logic NOT gate and the #2 CGL is equivalent to a basic tribotronic logic device. The V_A and V are the output signals of the #1 CGL and #2 CGL, respectively, which are logically complementary and also used as the input signals for the #3 CGL. The measured V_A is shown in Figure 6b, which has the reverse logic state with the input F_A. Therefore, the #3 CGL is equivalent to a basic tribotronic logic device when F_A is released, while a tribotronic logic NOT gate when F_A is applied, in which the output signal V_{out} can indicate the same or difference between the input F_A and F_B. With the exchanged ports for V_{bias} and ground, the tribotronic XNOR logic circuit has the similar structure. The inner signal V_A is measured in Figure 6f, which has the same logic state with the input F_A. Therefore, the output results of the tribotronic XOR and XNOR circuits will be logically complementary.

With these configurations, the measured output voltages at different combined states of input F_A and F_B, experimental truth table and logic symbol of the XOR gate are shown in Figure 6b–d, while the measurement results and logic symbol of the XNOR gate are shown in Figure 6f–h, which have realized the tribotronic XOR/XNOR logic operations with the CMOS logic level standard.

In summary, by using the triboelectric charges created by the contact electrification to modulate the charge carrier transportation in the conduction channel, the floating contact-electric-field gated tribotronic transistor has been proposed by coupling a silicon based field-effect transistor and a triboelectric nanogenerator. With the process of contact and separation between the mobile layer and floating gate, the CGT can be gated by an external force, which has the same effect as injecting charges on the floating gate in conventional transistor. With two opposite CGTs, the contact-gated tribotronic logic device has been fabricated to convert external mechanical stimuli into logic level signals. The output voltage of the CGL can be on-off switched by the external force, which has established the relationship between the mechanical force and CMOS logic electric level. By further assembling and integrating CGLs, universal combinational logic circuits, such as NOT, AND, OR, NAND, NOR, XOR, and XNOR gates, have been demonstrated for first performing mechanical–electrical coupled tribotronic logic operations. Different from the conventional logic units controlled by electrical signals, the contact-gated tribotronic

Adv. Mater. **2015**,
DOI: 10.1002/adma.201501511

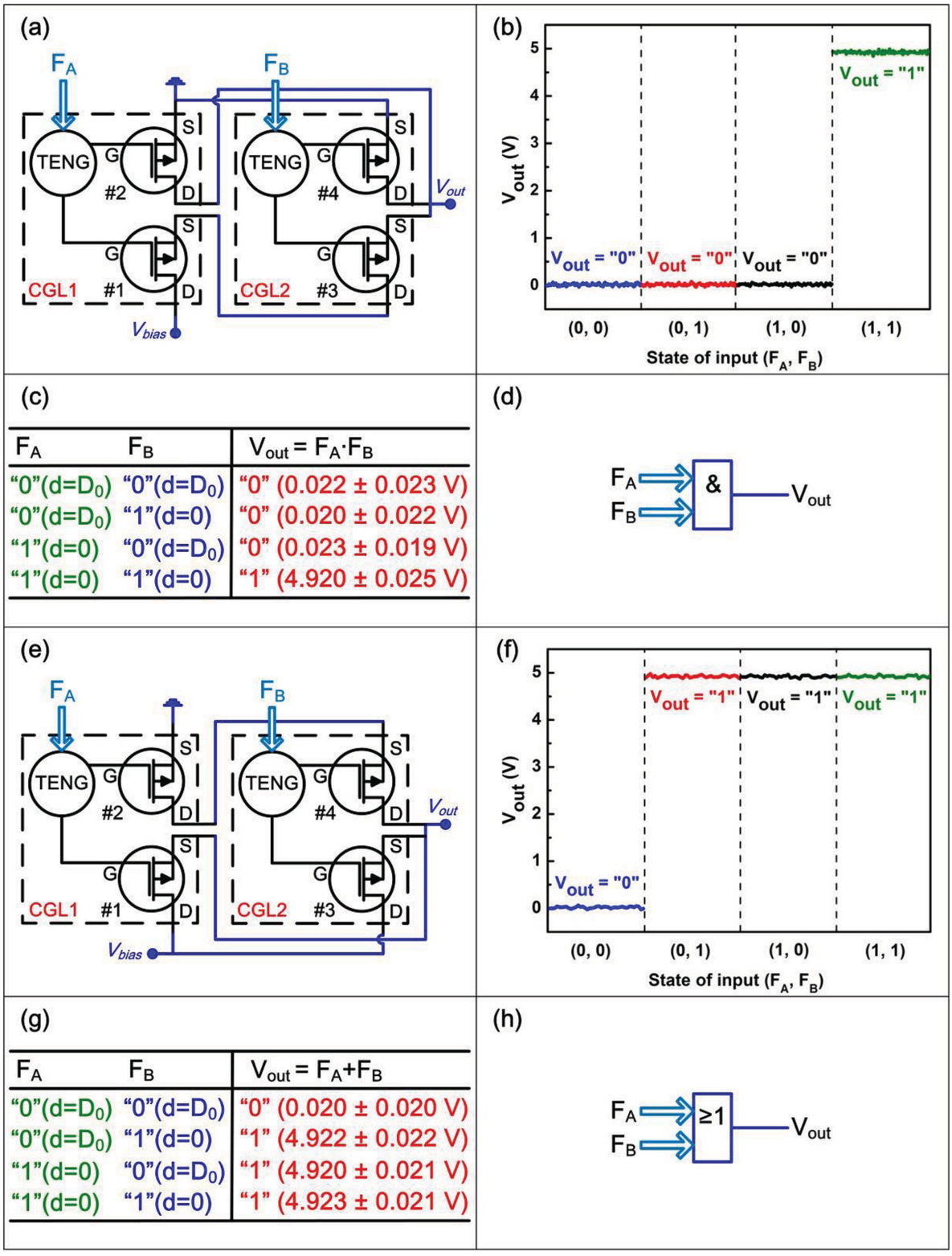

Figure 4. Contact-gated tribotronic logic AND and OR gates. a) Equivalent circuit of the AND gate based on two CGLs. b) The measured output voltages of the AND gate at different combined states of input F_A and F_B. c) Experimental truth table of the AND gate with physical values following each corresponding logic level. d) Logic symbol of the tribotronic logic AND gate. e) Equivalent circuit of the OR gate based on two CGLs. f) The measured output voltages of the OR gate at different combined states of input F_A and F_B. g) Experimental truth table of the OR gate with physical values following each corresponding logic level. h) Logic symbol of the tribotronic logic OR gate.

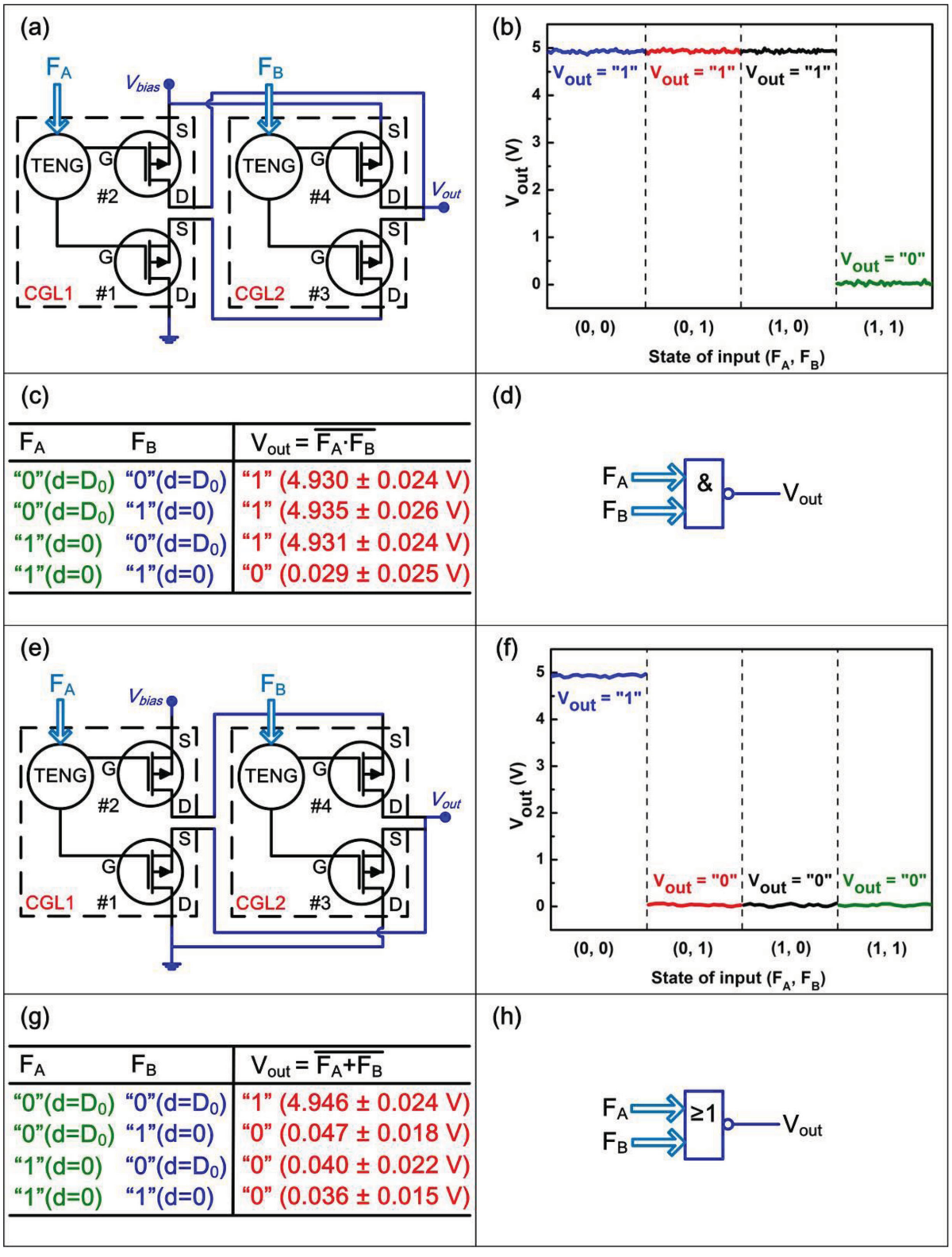

Figure 5. Contact-gated tribotronic logic NAND and NOR gates. a) Equivalent circuit of the NAND gate based on two CGLs. b) The measured output voltages of the NAND gate at different combined states of input F_A and F_B. c) Experimental truth table of the NAND gate with physical values following each corresponding logic level. d) Logic symbol of the tribotronic logic NAND gate. e) Equivalent circuit of the NOR gate based on two CGLs. f) The measured output voltages of the NOR gate at different combined states of input F_A and F_B. g) Experimental truth table of the NOR gate with physical values following each corresponding logic level. h) Logic symbol of the tribotronic logic NOR gate.

Adv. Mater. **2015**,
DOI: 10.1002/adma.201501511

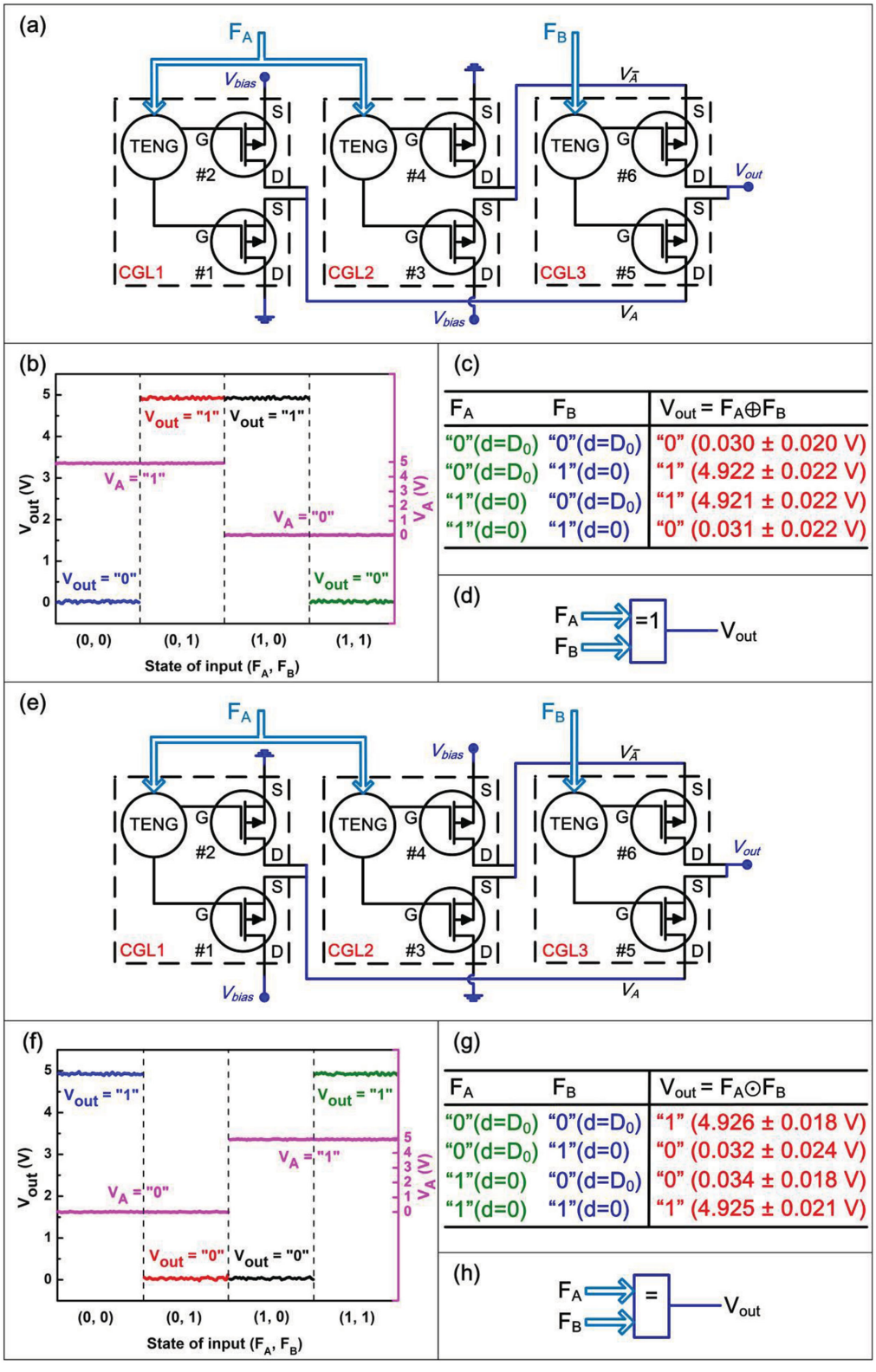

Figure 6. Contact-gated tribotronic logic XOR and XNOR gates. a) Equivalent circuit of the XOR gate based on three CGLs. b) The measured electrical output voltages of the XOR gate at different combined states of input F_A and F_B. c) Experimental truth table of the XOR gate with physical values following each corresponding logic level. d) Logic symbol of the tribotronic logic XOR gate. e) Equivalent circuit of the XNOR gate based on three CGLs. f) The measured electrical output voltages of the XNOR gate at different combined states of input F_A and F_B. g) Experimental truth table of the XNOR gate with physical values following each corresponding logic level. h) Logic symbol of the tribotronic logic XNOR gate.

logic units have realized the interaction between the external environment and the current silicon integrated circuits, which will be the foundation for further research on a new field of tribotronic digital circuits, such as trigger, sequential logic circuit, memory, etc. Compared with the existing passive sensors, such as capacitive and resistive types,[31,32] the demonstrated concept of tribotronic circuits and operations has provided an active sensing mode and may have great prospects in human-computer interaction, MEMS/NEMS, intelligent robots, and internet of things.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

C.Z. and L.M.Z. contributed equally to this work. The project was supported by National Natural Science Foundation of China (Grant Nos. 51475099 and 51432005), the "thousands talents" program for the pioneer researcher and his innovation team, China, and the Beijing Municipal Science & Technology Commission (Grant Nos. Z131100006013004 and Z131100006013005).

Received: March 30, 2015
Revised: April 15, 2015
Published online:

[1] R. Raussendorf, H. J. Briegel, *Phys. Rev. Lett.* **2001**, *86*, 5188.
[2] F. M. Raymo, *Adv. Mater.* **2002**, *14*, 401.
[3] H. Yan, H. S. Choe, S. W. Nam, Y. Hu, S. Das, J. F. Klemic, J. C. Ellenbogen, C. M. Lieber, *Nature* **2011**, *470*, 240.
[4] G. Zheng, W. Lu, S. Jin, C. M. Lieber, *Adv. Mater.* **2004**, *16*, 1890.
[5] Z. Chen, J. Appenzeller, Y. M. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon, P. Avouris, *Science* **2006**, *311*, 1735.
[6] A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker, *Science* **2001**, *294*, 1317.
[7] Y. M. Lin, A. Valdes-Garcia, S. J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, K. A. Jenkins, *Science* **2011**, *332*, 1294.
[8] R. Sordan, F. Traversi, V. Russo, *Appl. Phys. Lett.* **2009**, *94*, 073305.
[9] B. Radisavljevic, M. B. Whitwick, A. Kis, *ACS Nano* **2011**, *5*, 9934.
[10] H. Wang, L. Yu, Y. H. Lee, Y. Shi, A. Hsu, M. L. Chin, L. J. Li, M. Dubey, J. Kong, T. Palacios, *Nano Lett.* **2012**, *12*, 4674.
[11] Z. L. Wang, W. Wu, *Natl. Sci. Rev.* **2014**, *1*, 62.
[12] X. Wang, *Am. Ceram. Soc. Bull.* **2013**, *92*, 18.
[13] J. Shi, M. B. Starr, X. Wang, *Adv. Mater.* **2012**, *24*, 4683.
[14] Z. Zhang, Q. Liao, Y. Yu, X. Wang, Y. Zhang, *Nano Energy* **2014**, *9*, 237.
[15] Z. L. Wang, *Adv. Mater.* **2012**, *24*, 4632.
[16] R. Zhu, R. Yang, *Nanotechnology* **2014**, *25*, 345702.
[17] W. Wu, Y. Wei, Z. L. Wang, *Adv. Mater.* **2010**, *22*, 4711.
[18] R. Yu, W. Wu, Y. Ding, Z. L. Wang, *ACS Nano* **2013**, *7*, 6403.
[19] R. Yu, W. Wu, C. Pan, Z. Wang, Y. Ding, Z. L. Wang, *Adv. Mater.* **2015**, *27*, 940.
[20] F. R. Fan, Z. Q. Tian, Z. L. Wang, *Nano Energy* **2012**, *1*, 328.
[21] Z. L. Wang, *Faraday Discuss.* **2014**, *176*, 447.
[22] C. Zhang, W. Tang, C. B. Han, F. R. Fan, Z. L. Wang, *Adv. Mater.* **2014**, *26*, 3580.
[23] S. Kim, M. K. Gupta, K. Y. Lee, A. Sohn, T. Y. Kim, K. S. Shin, D. Kim, S. K. Kim, K. H. Lee, H. J. Shin, D. W. Kim, S. W. Kim, *Adv. Mater.* **2014**, *26*, 3918.
[24] C. Zhang, W. Tang, Y. K. Pang, C. B. Han, Z. L. Wang, *Adv. Mater.* **2015**, *27*, 719.
[25] C. Zhang, T. Zhou, W. Tang, C. B. Han, L. M. Zhang, Z. L. Wang, *Adv. Energy Mater.* **2014**, *4*, 1301798.
[26] X. S. Zhang, M. D. Han, R. X. Wang, B. Meng, F. Y. Zhu, X. M. Sun, W. Hu, W. Wang, Z. H. Li, H. X. Zhang, *Nano Energy* **2014**, *4*, 123.
[27] C. B. Han, C. Zhang, J. J. Tian, X. H. Li, L. M. Zhang, Z. Li, Z. L. Wang, *Nano Res.* **2014**, *8*, 219.
[28] C. B. Han, C. Zhang, W. Tang, X. H. Li, Z. L. Wang, *Nano Res.* **2014**, *8*, 722.
[29] W. Li, J. Sun, M. Chen, *Nano Energy* **2014**, *3*, 95.
[30] C. Zhang, W. Tang, L. M. Zhang, C. B. Han, Z. L. Wang, *ACS Nano* **2014**, *8*, 8702.
[31] Y. Zang, F. Zhang, D. Huang, X. Gao, C. Di, D. Zhu, *Nat. Commun.* **2015**, *6*, 6269.
[32] P. Ray, V. R. Rao, *Appl. Phys. Lett.* **2013**, *102*, 064101.