ACSNANO

www.acsnano.org

ARTICLE

Theoretical Study of Triboelectric-Potential Gated/Driven Metal–Oxide–Semiconductor Field-Effect Transistor

Wenbo Peng,[†,‡,⊥] Ruomeng Yu,[†,⊥] Yongning He,[‡] and Zhong Lin Wang[*,†,§]

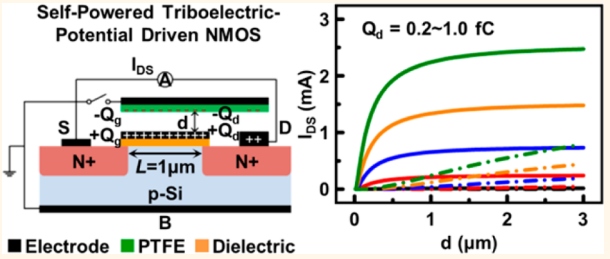
[†]School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332-0245, United States

[‡]School of Electronic and Information Engineering, Xi'an Jiaotong University, Xi'an 710049, China

[§]Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing 100083, China

Supporting Information

ABSTRACT: Triboelectric nanogenerator has drawn considerable attentions as a potential candidate for harvesting mechanical energies in our daily life. By utilizing the triboelectric potential generated through the coupling of contact electrification and electrostatic induction, the "tribotronics" has been introduced to tune/control the charge carrier transport behavior of silicon-based metal–oxide–semiconductor field-effect transistor (MOSFET). Here, we perform a theoretical study of the performances of tribotronic MOSFET gated by triboelectric potential in two working modes through finite element analysis. The drain-source current dependence on contact-electrification generated triboelectric charges, gap separation distance, and externally applied bias are investigated. The in-depth physical mechanism of the tribotronic MOSFET operations is thoroughly illustrated by calculating and analyzing the charge transfer process, voltage relationship to gap separation distance, and electric potential distribution. Moreover, a tribotronic MOSFET working concept is proposed, simulated and studied for performing self-powered FET and logic operations. This work provides a deep understanding of working mechanisms and design guidance of tribotronic MOSFET for potential applications in micro/nanoelectromechanical systems (MEMS/NEMS), human-machine interface, flexible electronics, and self-powered active sensors.



KEYWORDS: *triboelectric nanogenerator, field-effect transistor, tribotronics, self-powered*

The metal–oxide–semiconductor field-effect transistor (MOSFET) composed of an MOS capacitor and two adjacent p–n junctions is one of the most important units for forefront high-density integrated circuits that are the indispensible electronic building blocks of smartphone, computer and other microchip-enabled electronic devices. The carrier transport process as well as the drain-source current (I_{DS}) in the MOSFET is generally modulated by an externally applied gate voltage (V_{GS}).[1] Because of the lack of direct interaction between the external environment and electronic components such as MOSFET, transistors ordinarily act as readout elements for the detection of property changes in the pressure-sensitive materials induced by the external mechanical stimulation/triggering. Thus, approaches for developing a direct interface between electronics and external environment are highly desirable. In 2007, an emerging field of piezotronics was invented,[2] in which the piezoelectric polarization charge-induced inner-crystal piezoelectric potential is utilized to modulate the charge carrier transport in piezoelectric semiconductor materials with wurtzite and zincblende structures (such as ZnO, GaN, and CdS) as well as 2D materials (MoS_2) at the contacts.[3−8] Piezotronic strain-gated transistors and basic logic devices based on ZnO nanowires and GaN nanobelts have been realized, which convert the external mechanical stimulation into electronic controlling signals for performing piezotronic logic operations.[3,4] Recently, a large-scale array three-dimensional (3D) circuitry integration of vertical ZnO nanowire piezotronic transistors has been reported for active tactile imaging.[5] Moreover, these piezoelectric semiconductor materials can also be utilized to fabricate piezoelectric nanogenerators for harvesting mechanical energies.[9,10]

Since the first report on the triboelectric nanogenerator (TENG) in 2012,[11] it has drawn considerable attention as an effective approach to scavenge mechanical energies in our daily life such as human motion,[12−18] wind,[19] and raindrop[20] and to

Received: January 3, 2016
Accepted: April 14, 2016

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX–XXX

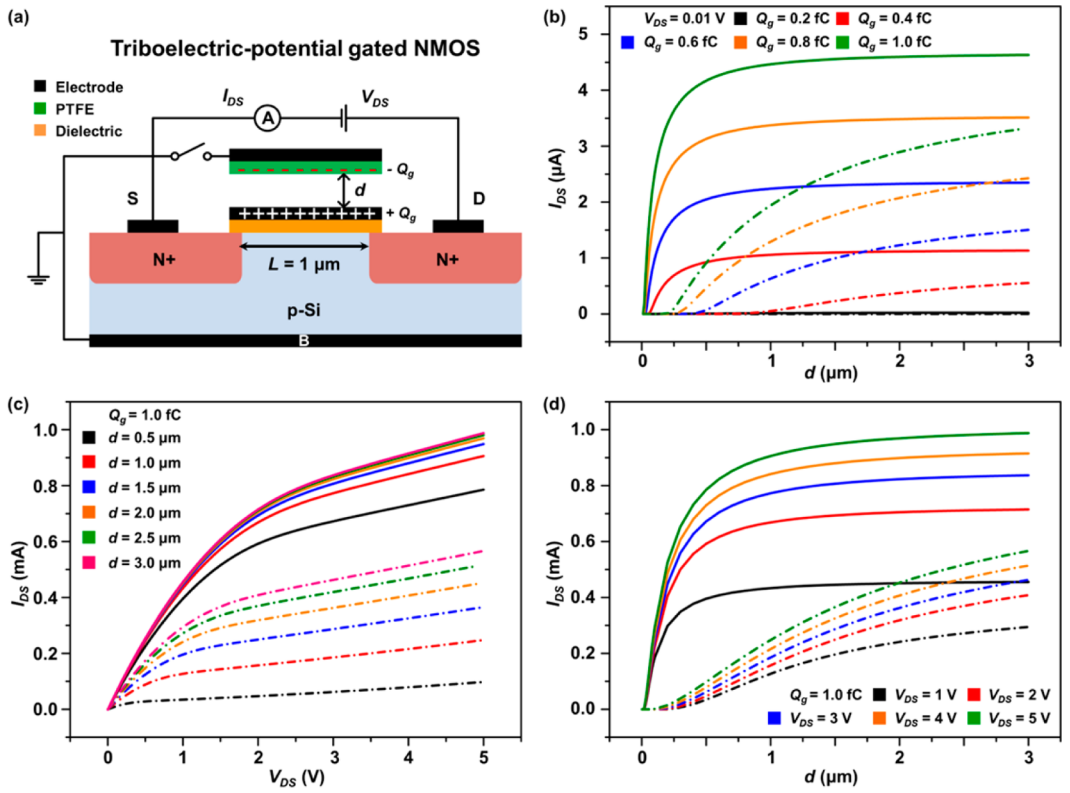


Figure 1. Triboelectric-potential gated (TPG) NMOS. (a) Schematic illustration of TPG NMOS, which is composed of a traditional silicon-based NMOS and a PTFE layer with aluminum electrode coated at its back as mobile electrode. (b) I_{DS}–d characteristic of TPG NMOS with a small V_{DS} bias of 0.01 V under different gate triboelectric charges (Q_g). (c) I_{DS}–V_{DS} output characteristic of TPG NMOS with Q_g of 1.0 fC under different d values from 0.5 to 3.0 μm. (d) I_{DS}–d characteristic of TPG NMOS with Q_g of 1.0 fC under different V_{DS} biases from 1 to 5 V.

act as self-powered sensors.[21,22] In addition, by utilizing the triboelectric-potential that is generated by contact induced triboelectric charges as the gate voltage to control/tune the charge carrier transport of transistor, a contact electrification field-effect transistor (CE-FET) was introduced, leading to a research field of tribotronics.[23] Most recently, through the coupling of a silicon-based MOSFET and a TENG, a floating contact-electric-field gated tribotronic transistor (CGT) and universal combinational logic circuits for mechanical-electrical coupled tribotronic logic operations have been demonstrated.[24] By contacting/separating the mobile polymer layer with/from the floating gate electrode, the CGT is gated by external force and the basic logic operations are realized through external mechanical stimuli, indicating huge potential in applications such as tribotronic digital circuits, memory, and fingerprint recognition. Here, we theoretically study the tribotronic MOSFETs powered by triboelectric-potential based on two fundamental working modes and concepts through finite element analysis (FEA), providing in-depth understanding of working mechanisms and design guidance for potential applications in micro/nano-electromechanical systems (MEMS/NEMS), human-machine interface, flexible electronics, and self-powered active sensors.

RESULTS AND DISCUSSION

The tribotronic MOSFET model built in the FEA is composed of a traditional silicon-based n-channel MOSFET (NMOS) for simplification and a polytetrafluoroethylene (PTFE) layer (25 nm in thickness) with aluminum (Al) electrode coated at its back as the mobile electrode, as schematically illustrated in Figure 1a. The conduction channel length (L) is 1 μm and the gate dielectric layer that overlaps the two heavily doped n-type regions has a length of 1.5 μm and a thickness of 20 nm. The distance between the PTFE layer and the gate electrode (d) varies from 1 nm to 3 μm. Other parameters of the NMOS such as doping concentration, doping profile, and detailed geometrical parameters can be found in Methods. The basic current–voltage (I–V) characteristics of the NMOS (Figure S1, Supporting Information) indicates the threshold voltage V_{th} of about 0.8 V and general I_{DS}–V_{DS} and I_{DS}–V_{GS} properties. Because the PTFE layer is in vertical alignment and contacts only with the gate electrode in this working concept, we define it as triboelectric-potential gated (TPG) NMOS.

The fundamental working mechanism of the TPG NMOS is based on the coupling of contact electrification, electrostatic induction, and basic silicon-based NMOS operations. At first, the PTFE layer is brought into fully physical contact with the gate electrode by external force/pressure, generating equal triboelectric charges in opposite polarities by contact electrification on PTFE layer and gate electrode, respectively. The PTFE layer is negatively charged and the gate electrode is positively charged according to the triboelectric series. As it releases the external force/pressure, the PTFE layer gradually separates from the gate electrode by a distance d with air dielectric between the two layers. Then an electric field and a potential drop are created due to the electrostatic induction, resulting in a built-in voltage at the gate electrode to tune/control the charge carrier transport properties between the drain and source electrodes. When the distance d increases to a specific value as the threshold distance d_{th}, the triboelectric charges induced gate voltage reaches the threshold voltage V_{th},

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX–XXX

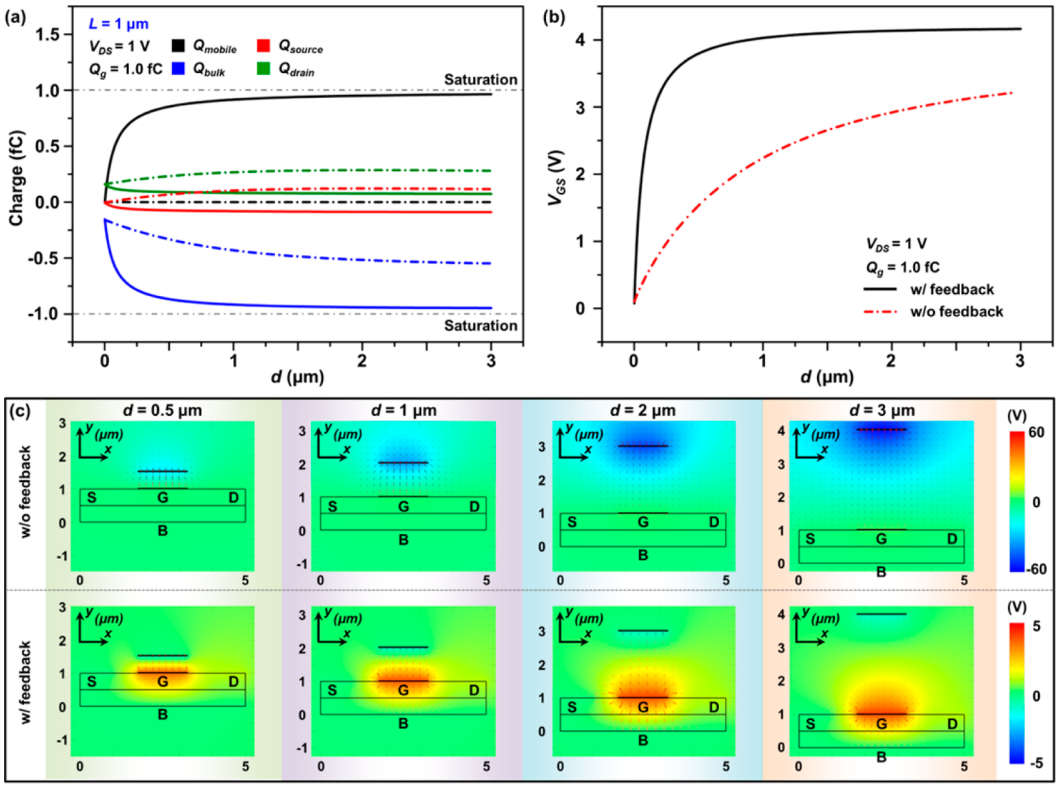


Figure 2. Charge transfer, induced gate voltage (V_{GS}), electric potential and electric field distribution of TPG NMOS with V_{DS} bias of 1 V and Q_g of 1.0 fC. (a) Total charge amounts of all four electrodes and (b) triboelectric charges electrostatically induced V_{GS} with d ranging from 1 nm to 3 μm. (c) Electric potential and electric field (red arrows) distribution with different d values: 0.5, 1, 2, and 3 μm.

creating an inversion conduction channel between drain and source underlying the gate dielectric and, thus, producing the drain-source current I_{DS} by applying a drain voltage (V_{DS}), turning the NMOS "on". Further release of external force/pressure is similar to increasing the applied gate voltage, which decreases the resistance of the conduction channel and increases I_{DS}. Here, we consider two working modes: one is that the mobile electrode is connected to the grounded source and bulk electrodes; the other one is that the mobile electrode is isolated from all other electrodes as a "floating" one. On the basis of the presence/absence of feedback charges from outside the mobile electrode during operations that is analogous to the "short-circuit" and the "open-circuit" conditions of TENG, these two working modes are defined as "w/feedback" and "w/o feedback", respectively.

The dependence of threshold distance d_{th} on the amount of contact electrification generated triboelectric charges on gate electrode (Q_g) is simulated first by varying the separated distance d between PTFE layer and gate electrode from 1 nm to 3 μm with a small V_{DS} bias of 0.01 V, as illustrated in Figure 1b. Under "w/o feedback" mode (dash−dot lines in Figure 1b; dash−dot lines in the following article represent "w/o feedback" mode unless otherwise specified), I_{DS} first keeps almost zero ("off" state) and then increases gradually ("on" state) after d reaches a specific value d_{th}, showing a similar turning on process to silicon-based NMOS. However, under "w/feedback" mode (solid lines in Figure 1b; solid lines in the following article represent "w/feedback" mode unless otherwise specified), TPG NMOS turns on at a very small d value, and I_{DS} increases dramatically to saturation, which is totally different from the "w/o feedback" mode. Besides, under both modes, I_{DS} exhibits a saturation trend when d increases, with a fast saturation in "w/feedback" mode and a slow saturation in "w/o feedback" mode, which differs from silicon-based NMOS (Figure S1b, Supporting Information). Moreover, as shown in Figure 1b, d_{th} of both modes decreases as Q_g increases because the larger the Q_g, the stronger the electrostatic induction effect. Besides, at Q_g = 0.2 fC, TPG NMOS retains at "off" state for both modes, indicating a minimum Q_g required for turning on the device.

Other transmission characteristics of TPG NMOS including I_{DS}−V_{DS} at different d values and I_{DS}−d at different V_{DS} values are simulated by fixing Q_g at 1.0 fC, as illustrated in Figure 1c,d. At each fixed d value (ranging from 0.5 to 3.0 μm), I_{DS} presents a two-stage increase behavior under both w/and w/o feedback modes (Figure 1c): I_{DS} increases with a sharp slope initially and then with a shallow slope, showing no saturation as increasing V_{DS}. Different from TPG NMOS, I_{DS} of traditional Si-based NMOS generally increases to saturation disregarding the reduced effective channel length caused by applying V_{DS} bias beyond $V_{DSsat} = V_{GS} - V_{th}$ if the channel length is much larger than the change of channel length. However, for those whose channel length is small, the reduced amount of effective channel length is a substantial fraction of the channel length and this will increase I_{DS} even the NMOS works in the saturation region, which is also named as short-channel effect. Therefore, the I_{DS}−V_{DS} characteristic of TPG NMOS could be regarded as a short-channel silicon-based NMOS, although the NMOS in our model has a large channel length of 1 μm and does not show clear I_{DS} increase in the saturation region (Figure S1c, Supporting Information). When biased with V_{DS} from 1 to 5 V, TPG NMOS represents totally different I_{DS}−d characteristics under two modes (Figure 1d): the I_{DS} of "w/o feedback" mode increases gradually with d, similar as the I_{DS}−V_{GS} characteristic

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX−XXX

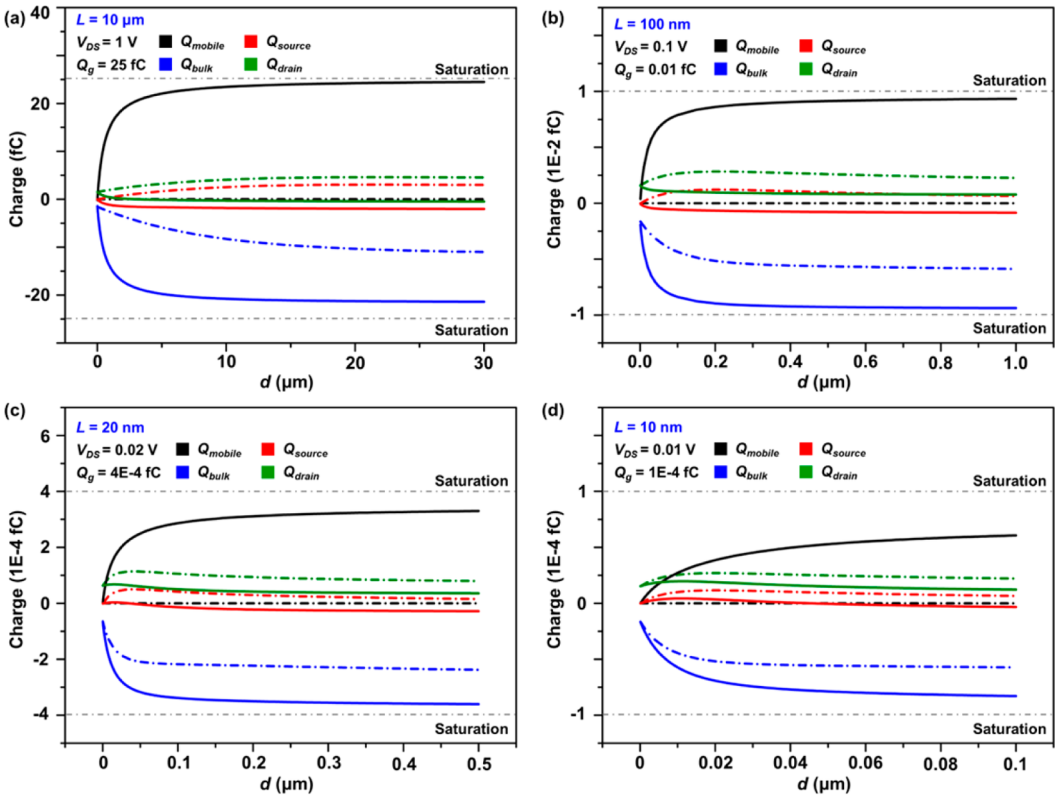


Figure 3. Charge transfer of TPG NMOS with conduction channel length (L) of (a) 10 μm, (b) 100 nm, (c) 20 nm, and (d) 10 nm. While L scales up/down, all the parameters related to the NMOS also scale up/down, meaning the fully scaling.

of silicon-based NMOS (Figure S 1d, Supporting Information), whereas the I_{DS} of "w/feedback" mode first increases quickly and gradually reaches a saturation.

To better understand the physical mechanism of the different I_{DS}–d behavior of TPG NMOS under two working modes, total charge amount of all four electrodes, including mobile (Q_{mobile}), source (Q_{source}), bulk (Q_{bulk}), and drain (Q_{drain}) electrodes, and triboelectric charge-induced gate voltage (V_{GS}) versus separated distance d under two modes are calculated with bias V_{DS} of 1 V and Q_g of 1.0 fC, as illustrated in Figure 2a,b. For "w/o feedback" mode, the Q_{mobile} remains zero with d increasing from 1 nm to 3 μm because that the mobile electrode is isolated from all other electrodes as a "floating" one. With d increases, the built-in potential drop from the gate electrode to the PTFE layer increases, thus leading to an increase of the absolute value of Q_{source}, Q_{bulk}, and Q_{drain} in order to keep the externally applied potential on these three electrodes constant. As a result of the increase of absolute total charge amounts, the triboelectric charge-induced V_{GS} increases as well (Figure 2b). Electric potential and electric field distribution at different d values: 0.5, 1, 2, and 3 μm at "w/o feedback" mode (Figure 2c, top panel) also indicates that the built-in potential drop from gate electrode to PTFE layer increases with d and electric field is mainly distributed between gate electrode and PTFE layer because Q_{source}, Q_{bulk}, and Q_{drain} are far away from saturation (gray dash-dot line in Figure 2a, indicating the maximum transferred charge amount Q_g). As for the "w/feedback" mode, upon separating PTFE layer from gate electrode, a built-in electric field forms, driving electrons flow from mobile electrode to all other three electrodes, which is similar to the short-circuit condition of TENG. The charge transfer process is almost completed instantaneously upon the separation of PTFE layer from gate electrode and reaches a steady condition rapidly as the Q_{mobile} approaches to Q_g quickly. Consequently, the triboelectric charge-induced V_{GS} increases dramatically to the saturation. Furthermore, as illustrated in bottom panel of Figure 2c, the electric potential distribution remains almost unchanged with d varying from 0.5 to 3 μm. This different V_{GS}–d characteristic between two working modes arising from the presence/absence of charge transfer among four electrodes is responsible for the totally different I_{DS}–d behavior as shown in Figure 1d.

By scaling down conduction channel length L of the NMOS in the model from 10 μm to 10 nm, the device size dependence of the charge transfer process of TPG NMOS under two modes is simulated and investigated as shown in Figure 3. While L scales up/down from 1 μm, all the parameters of silicon-based NMOS—including conduction channel width and all other device geometric parameters, gate dielectric layer's thickness, applied bias voltages, silicon substrate's doping concentration, and source/drain doping profile—also scale up/down proportionally. Besides, the thickness of PTFE layer and the generated triboelectric surface charge density keep unchanged considering that the contact electrification process between PTFE layer and gate electrode remains the same. For "w/o feedback" mode with L of 10 μm, 100 nm, 20 and 10 nm, Q_{mobile} keeps zero and Q_{source}, Q_{bulk}, and Q_{drain} changes gradually as d increases, showing a similar charge transfer process to that of L = 1 μm. This is further confirmed by the calculated results of I_{DS}–d, I_{DS}–V_{DS}, and V_{GS}–d characteristics and electric potential and electric field distributions with L = 10 μm, 100 nm, and 10 nm (Figures S2, S4, and S6, Supporting Information).

However, for "w/feedback" mode, the charge transfer processes at L = 10 μm, 100 nm, 20 nm, and 10 nm present

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX–XXX

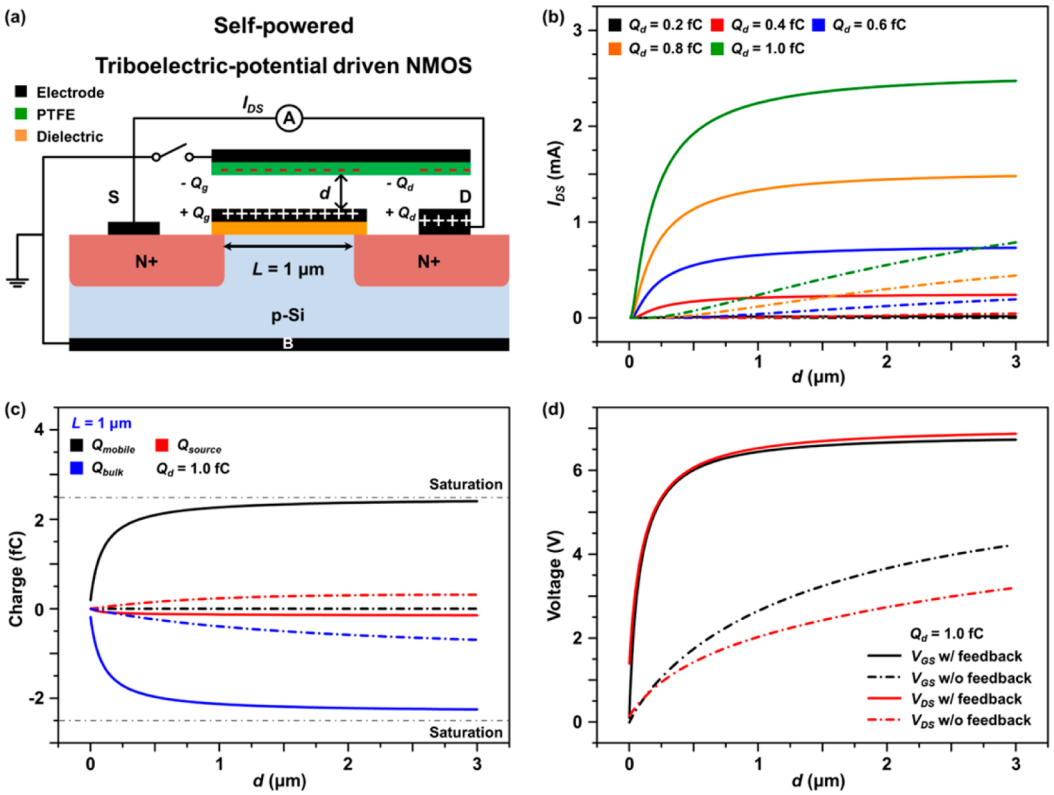


Figure 4. Self-powered triboelectric-potential driven (TPD) NMOS. (a) Schematic illustration of TPD NMOS, where PTFE layer contacts both gate and drain electrodes for contact electrification. (b) I_{DS}–d characteristic under different Q_d values from 0.2 to 1.0 fC. (c) Charge transfer and (d) triboelectric charges induced V_{GS} and V_{DS} with Q_d of 1.0 fC and d ranging from 1 nm to 3 μm.

different behaviors as shown in Figure 3 (solid lines). As L is much larger than the thickness of PTFE layer (L = 10 μm, 100 nm), the charge transfer process (Figure 3a,b), the corresponding I_{DS}–d, I_{DS}–V_{DS}, V_{GS}–d characteristics and electric potential and electric field distributions (Figure S2 and S4, Supporting Information) are similar to that at L = 1 μm (Figure 2a). At L = 10 nm, which is smaller than the thickness of PTFE layer (25 nm), the charge transfer process (Figure 3d) becomes inefficient compared with that of L = 10 μm, 1 μm, and 100 nm. Also, Q_{mobile} increases gradually without saturating other than saturates rapidly (Figures 2a and 3a,b). Accordingly, the I_{DS}–d, I_{DS}–V_{DS}, and V_{GS}–d characteristics, electric potential, and electric field distributions (Figure S6, Supporting Information) show the similar trend as the charge transfer process (Figure 3d). At L = 20 nm which is comparable to the thickness of PTFE layer, the charge transfer process (Figure 3c) shows a transitional-behavior from the rapid transfer process (Figure 2a) to the slow one (Figure 3d) with Q_{mobile} increasing quickly to about three-quarters of Q_g. Therefore, for transistors with size much larger than the thickness of mobile polymer layer for contact electrification, the two working modes of TPG NMOS show different characteristics and, thus, can be utilized in different applications, whereas for transistors with size smaller than the thickness of mobile polymer layer for contact electrification, the two working modes of TPG NMOS are almost the same.

As described above, TPG NMOS utilizes the triboelectric charges induced potential to serve as the gate voltage for tuning/controlling the charge carrier transport between drain and source electrodes, where an externally applied bias V_{DS} is still needed. By bringing the PTFE layer into physical contact with both gate and drain electrodes, the triboelectric charges induced potential serves as the gate voltage V_{GS} and externally applied bias V_{DS} simultaneously, indicating a working concept defined as self-powered triboelectric-potential driven (TPD) NMOS, as schematically illustrated in Figure 4a. All of the parameters of silicon-based NMOS and the thickness of PTFE layer are the same, except that the length of the PTFE layer is increased to vertically align and contact with both gate and drain electrodes. Because gate and drain electrodes are both Al, the contact electrification between PTFE layer and these two electrodes should be the same. Thus, it is assumed that the generated triboelectric surface charge density is the same on gate and drain electrodes. We only define the total charge amount of drain electrode (Q_d), and then Q_g can be calculated through the ratio of gate electrode area to drain electrode area.

The transmission characteristic of TPD NMOS is simulated by varying Q_d from 0.2 fC to 1.0 fC, as shown in Figure 4b. Under "w/o feedback" mode, TPD NMOS turns on at a specific separated distance d_{th}, and I_{DS} increases linearly with no saturation observed. While under "w/feedback" mode, TPD NMOS turns on instantaneously upon the separation of PTFE layer from gate and drain electrodes, and I_{DS} increases linearly at initial stage and then reaches saturation gradually. The differences between two modes are contributed to the different charge transfer process as illustrated in Figure 4c. Similar to TPG NMOS, Q_{mobile} of TPD NMOS also remains zero under "w/o feedback" mode with Q_{source} and Q_{bulk} gradually changing in order to keep source and bulk electrodes grounded, whereas under "w/feedback" mode, Q_{mobile} increases quickly to saturation (Q_d + Q_g) due to the electron flow from mobile electrode to source and bulk electrodes driven by the built-in

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX–XXX

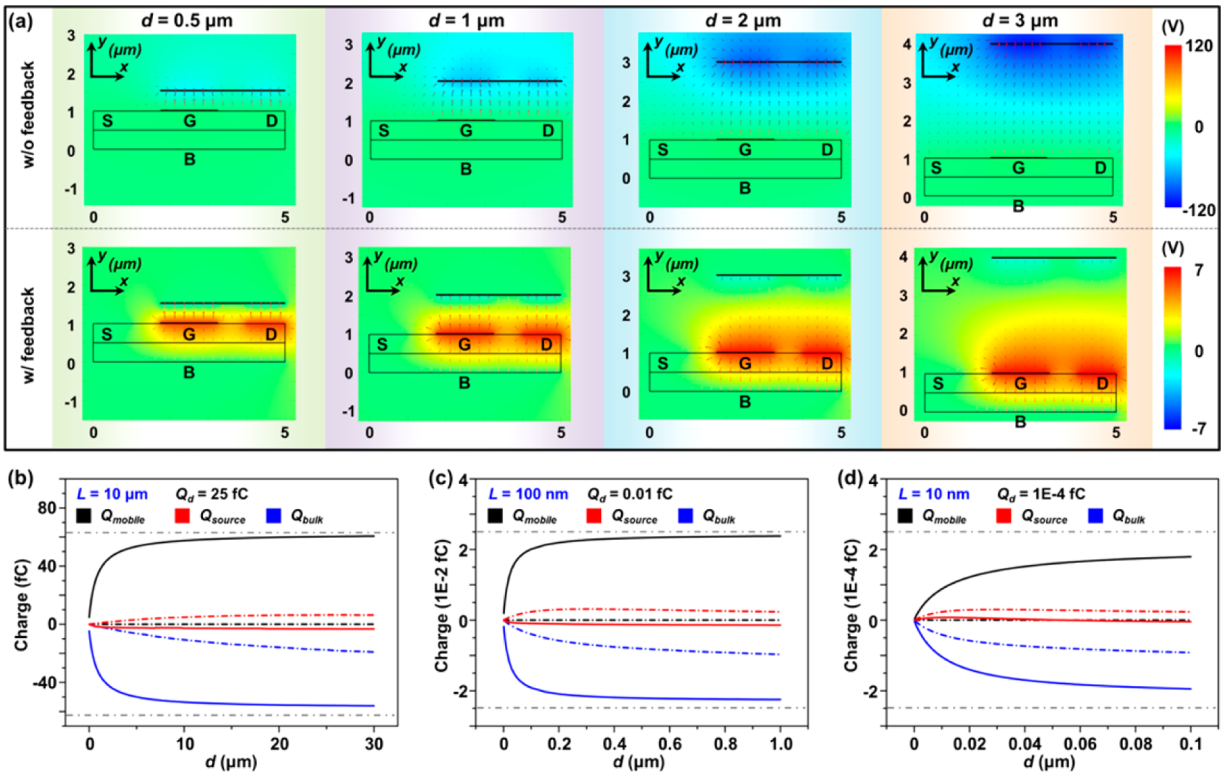


Figure 5. (a) **Electric potential and electric field distribution of TPD NMOS with Q_d of 1.0 fC and different d values: 0.5, 1, 2, and 3 μm. (b–d) Charge transfer characteristics of TPD NMOS with conduction channel length L scaling up/down from 10 μm to 10 nm.**

electric field between PTFE layer and gate and drain electrodes. Thus, the negative triboelectric charges on PTFE layer are almost electrostatically screened and the triboelectric charges induced V_{GS} and V_{DS} increase quickly to saturation (Figure 4d). As illustrated by Figure 5a, under "w/o feedback" mode, the electric potential drop from gate/drain electrode to PTFE layer increases with d ranging from 0.5 to 3 μm, and the electric field mainly distributes between PTFE layer and gate/drain electrode (Figure 5a, top panel). However, under "w/feedback" mode, the electric potential distribution remains almost unchanged when d increases from 0.5 to 3 μm (Figure 5a, bottom panel). Consequently, the electric field between PTFE layer and gate/drain electrode gradually weakens with the electric field inside silicon substrate enhancing due to increased d.

The device size dependence of the charge transfer process of TPD NMOS under two working modes is also simulated and investigated, as shown in Figure 5b–d. For "w/o feedback" mode, all the charge transfer processes as well as the I_{DS}–d, V_{GS}–d, and V_{DS}–d characteristics (Figures S3, S5, and S7, Supporting Information) are similar to that of L = 1 μm. However, for "w/feedback" mode, when L is larger than the thickness of PTFE layer (L = 10 μm and 100 nm), charge transfers quickly to the saturation as the same as that for L = 1 μm condition. When L is smaller than the thickness of PTFE layer (L = 10 nm), charge transfers slowly without saturation. Moreover, the I_{DS}–d, V_{GS}–d and V_{DS}–d characteristics of "w/feedback" mode (Figures S3, S5, and S7, Supporting Information) further verify this transition from fast charge transfer process to slow charge transfer process.

Both the TPG NMOS and the self-powered TPD NMOS under "w/feedback" mode with conduction channel length L = 1 μm possess rapid switching speed upon separating the mobile PTFE layer, indicating the potential to operate as fast electromechanical switch controlled by environmental mechanical stimuli. The switching speed of these tribotronic devices is mainly determined by two factors: (i) the intrinsic switching speed of the electronic transistor itself and (ii) the speed of applying external stimuli to the devices. The switching delay of modern electronic transistors is generally at the nanosecond scale, meaning a very fast switch in the GHz range. However, because the control signal (i.e., the gate voltage V_{GS}) is produced by external stimuli, such as human motions and environmental vibrations, which are typically in the kilohertz range, the switching speed of the whole tribotronic devices as electromechanical switch is dominated by the external stimuli and is at the millisecond scale.

In practical applications, electrostatic discharge (ESD) is a major concern in advanced MOSFETs. Because the tribotronic devices utilize the triboelectric contact electrification and electrostatic induction to produce the gate voltage V_{GS}, it is essential to avoid possible ESD failures. Detailed discussion about the ESD solution is found in the Supporting Information Note 1. Moreover, in a real MOSFET, carrier mobility degrades with phonons, impurities, surface roughness scattering, and electric field. The carrier mobility degradation due to these effects are carefully simulated and discussed in the Supporting Information Note 2. The results show that the current I_{DS} is reduced significantly for both TPG NMOS and self-powered TPD NMOS under two working modes. Whereas the I_{DS}–V_{DS} and the I_{DS}–d correlations remain unchanged, indicating that the carrier mobility degradation has no effects on the operation of tribotronic devices.

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX–XXX

CONCLUSIONS

In summary, we have carried out theoretical study of tribotronic MOSFETs by FEA. For TPG NMOS where the triboelectric-potential serves as the gate voltage, the transistor under "w/o feedback" mode operates as a general short-channel silicon-based NMOS; the transistor under "w/feedback" mode is similar to electromechanical switch with quick switching between "on" and "off" states by separating the PTFE layer from gate electrodes for a short distance (hundreds of nanometers). For TPD NMOS in which triboelectric-potential serves as both the gate and drain voltages, the transistor under "w/o feedback" mode is similar to a general NMOS; the transistor under "w/feedback" mode performs as a self-powered electromechanical switch. The achieved different operating behavior under two working modes is attributed to the absence/presence of charge transfer process between mobile electrode and other electrodes. Our simulated results also indicate that for both TPG and TPD NMOS under "w/feedback" mode, the fast charge transfer process between mobile electrode and other electrodes transit to a slow process as device size scaling down to smaller than the thickness of PTFE layer. This work provides in-depth understanding of the physical mechanism of tribotronic MOSFETs in two basic working modes and two working concepts, showing a great potential in fingerprint recognition, self-powered electronics, flexible/wearable electronics, and human−machine interfaces.

METHODS

Tribotronic MOSFET Model Development: All the simulations in this study are performed by utilizing the semiconductor module in COMSOL Multiphysics software. The NMOS device model in the simulation has a length of 5 μm, width of 1 μm and thickness of 1 μm. The background p-type doping concentration of silicon substrate is 10^{17} cm^{-3} and the uniform n-type heavily doping concentration for drain/source is 10^{20} cm^{-3} with width of 1.6 μm and thickness of 0.1 μm. The doping profile away from the uniform region is defined by the junction depth (d_j) toward each direction utilizing a Gaussian decay function, with d_j toward the length direction of 0.3 μm and the thickness direction of 0.45 μm. Both the drain and source electrodes are 1 μm long and 1 μm wide. The bulk electrode is 5 μm long and 1 μm wide, same as the bottom boundary of NMOS device. The gate dielectric layer partly overlaps two heavily doped regions is 1.5 μm in length, 1 μm in width, and 20 nm in thickness, with a relative permittivity of 4.5. The gate electrode has the same length and width as gate dielectric layer. To be in vertical alignment with the gate electrode, the PTFE layer is also 1.5 μm long, 1 μm wide, and 25 nm thick and separated from the gate electrode with distance d varying in the simulation. The source and bulk electrodes are grounded. The drain electrode is biased with V_{DS} in TPG NMOS simulation and with electrostatically induced potential in TPD NMOS simulation. Both in TPG and TPD NMOS simulation, the gate electrode is biased with electrostatically induced potential. The PTFE layer and the NMOS are surrounded by air dielectric, and the contact electrification generated triboelectric charges on gate electrode in TPG NMOS simulation and on gate/drain electrode in TPD NMOS simulation are defined as Q_g and Q_g/Q_d respectively. The relative permittivity of air and PTFE are 1 and 2, respectively. For semiconductor material silicon, relative permittivity is 11.7, band gap 1.12 eV, electron affinity 4.05 eV, valence band effective density of states at room temperature (RT) 1.04×10^{19} cm^{-3}, conduction band effective density of states at RT 2.8×10^{19} cm^{-3}, electron mobility 1450 cm^2 V^{-1} s^{-1}, hole mobility 500 cm^2 V^{-1} s^{-1}, electron lifetime for Shockley−Read−Hall (SRH) recombination model 10 μs, and hole lifetime for SRH recombination model 10 μs. A trap-assisted recombination defined by SRH recombination model is applied to silicon to describe the recombination process. The NMOS is modeled by a conventional drift-diffusion approach using partial differential equations available internally within the semiconductor module in COMSOL. After the computation, by integrating the surface charge density on electrodes, the total amount of charges on all electrodes and, thus, the charge transfer process can be derived.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b00021.

More detailed information about traditional silicon-based NMOS; TPG and TPD NMOS with L of 10 μm, 100 nm, and 10 nm; electrostatic discharge problem; carrier mobility degradation. (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: zhong.wang@mse.gatech.edu.

Author Contributions

$^{\perp}$(W.P. and R.Y.) These authors contributed equally to this work.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This research was supported by U.S. Department of Energy, Office of Basic Energy Sciences (Award DE-FG02-07ER46394). W.P. would like to thank for the support from China Scholarship Council (CSC).

REFERENCES

(1) Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.

(2) Wang, Z. L. Nanopiezotronics. *Adv. Mater.* **2007**, *19*, 889−892.

(3) Wu, W. Z.; Wei, Y. G.; Wang, Z. L. Strain-Gated Piezotronic Logic Nanodevices. *Adv. Mater.* **2010**, *22*, 4711−4715.

(4) Yu, R. M.; Wu, W. Z.; Ding, Y.; Wang, Z. L. GaN Nanobelt-Based Strain-Gated Piezotronic Logic Devices and Computation. *ACS Nano* **2013**, *7*, 6403−6409.

(5) Wu, W. Z.; Wen, X. N.; Wang, Z. L. Taxel-Addressable Matrix of Vertical-Nanowire Piezotronic Transistors for Active and Adaptive Tactile Imaging. *Science* **2013**, *340*, 952−957.

(6) Wu, W. Z.; Wang, Z. L. Piezotronic Nanowire-Based Resistive Switches as Programmable Electromechanical Memories. *Nano Lett.* **2011**, *11*, 2779−2785.

(7) Wu, W. Z.; Wang, L.; Li, Y. L.; Zhang, F.; Lin, L.; Niu, S. M.; Chenet, D.; Zhang, X.; Hao, Y. F.; Heinz, T. F.; Hone, J.; Wang, Z. L. Piezoelectricity of Single-Atomic-Layer MoS_2 for Energy Conversion and Piezotronics. *Nature* **2014**, *514*, 470−474.

(8) Yu, R. M.; Wu, W. Z.; Pan, C. F.; Wang, Z. N.; Ding, Y.; Wang, Z. L. Piezo-Phototronic Boolean Logic and Computation Using Photon and Strain Dual-Gated Nanowire Transistors. *Adv. Mater.* **2015**, *27*, 940−947.

(9) Lee, M.; Chen, C. Y.; Wang, S.; Cha, S. N.; Park, Y. J.; Kim, J. M.; Chou, L. J.; Wang, Z. L. A Hybrid Piezoelectric Structure for Wearable Nanogenerators. *Adv. Mater.* **2012**, *24*, 1759−1764.

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX−XXX

(10) Chen, C. Y.; Zhu, G.; Hu, Y. F.; Yu, J. W.; Song, J. H.; Cheng, K. Y.; Peng, L. H.; Chou, L. J.; Wang, Z. L. Gallium Nitride Nanowire Based Nanogenerators and Light-Emitting Diodes. *ACS Nano* **2012**, *6*, 5687−5692.
(11) Fan, F. R.; Tian, Z. Q.; Wang, Z. L. Flexible Triboelectric Generator. *Nano Energy* **2012**, *1*, 328−334.
(12) Cheng, X. L.; Meng, B.; Zhang, X. S.; Han, M. D.; Su, Z. M.; Zhang, H. X. Wearable Electrode-Free Triboelectric Generator for Harvesting Biomechanical Energy. *Nano Energy* **2015**, *12*, 19−25.
(13) Zhang, X. S.; Han, M. D.; Wang, R. X.; Zhu, F. Y.; Li, Z. H.; Wang, W.; Zhang, H. X. Frequency-Multiplication High-Output Triboelectric Nanogenerator for Sustainably Powering Biomedical Microsystems. *Nano Lett.* **2013**, *13*, 1168−1172.
(14) Kim, K. N.; Chun, J.; Kim, J. W.; Lee, K. Y.; Park, J. U.; Kim, S. W.; Wang, Z. L.; Baik, J. M. Highly Stretchable 2D Fabrics for Wearable Triboelectric Nanogenerator under Harsh Environments. *ACS Nano* **2015**, *9*, 6394−6400.
(15) Seung, W.; Gupta, M. K.; Lee, K. Y.; Shin, K. S.; Lee, J. H.; Kim, T. Y.; Kim, S.; Lin, J.; Kim, J. H.; Kim, S. W. Nanopatterned Textile-Based Wearable Triboelectric Nanogenerator. *ACS Nano* **2015**, *9*, 3501−3509.
(16) Jeong, C. K.; Baek, K. M.; Niu, S. M.; Nam, T. W.; Hur, Y. H.; Park, D. Y.; Hwang, G. T.; Byun, M.; Wang, Z. L.; Jung, Y. S.; Lee, K. J. Topographically-Designed Triboelectric Nanogenerator *via* Block Copolymer Self-Assembly. *Nano Lett.* **2014**, *14*, 7031−7038.
(17) Kim, S.; Gupta, M. K.; Lee, K. Y.; Sohn, A.; Kim, T. Y.; Shin, K. S.; Kim, D.; Kim, S. K.; Lee, K. H.; Shin, H. J.; Kim, D. W.; Kim, S. W. Transparent Flexible Graphene Triboelectric Nanogenerators. *Adv. Mater.* **2014**, *26*, 3918−3925.
(18) Hwang, B. U.; Lee, J. H.; Trung, T. Q.; Roh, E.; Kim, D. I.; Kim, S. W.; Lee, N. E. Transparent Stretchable Self-Powered Patchable Sensor Platform with Ultrasensitive Recognition of Human Activities. *ACS Nano* **2015**, *9*, 8801−8810.
(19) Bae, J.; Lee, J.; Kim, S.; Ha, J.; Lee, B. S.; Park, Y.; Choong, C.; Kim, J. B.; Wang, Z. L.; Kim, H. Y.; Park, J. J.; Chung, U. I. Flutter-Driven Triboelectrification for Harvesting Wind Energy. *Nat. Commun.* **2014**, *5*, 4929.
(20) Liang, Q. J.; Yan, X. Q.; Gu, Y. S.; Zhang, K.; Liang, M. Y.; Lu, S. N.; Zheng, X.; Zhang, Y. Highly Transparent Triboelectric Nanogenerator for Harvesting Water-Related Energy Reinforced by Antireflection Coating. *Sci. Rep.* **2015**, *5*, 9080.
(21) Han, M. D.; Zhang, X. S.; Sun, X. M.; Meng, B.; Liu, W.; Zhang, H. X. Magnetic-Assisted Triboelectric Nanogenerators as Self-Powered Visualized Omnidirectional Tilt Sensing System. *Sci. Rep.* **2014**, *4*, 4811.
(22) Ha, M.; Park, J.; Lee, Y.; Ko, H. Triboelectric Generators and Sensors for Self-Powered Wearable Electronics. *ACS Nano* **2015**, *9*, 3421−3427.
(23) Zhang, C.; Tang, W.; Zhang, L. M.; Han, C. B.; Wang, Z. L. Contact Electrification Field-Effect Transistor. *ACS Nano* **2014**, *8*, 8702−8709.
(24) Zhang, C.; Zhang, L. M.; Tang, W.; Han, C. B.; Wang, Z. L. Tribotronic Logic Circuits and Basic Operations. *Adv. Mater.* **2015**, *27*, 3533−3540.

DOI: 10.1021/acsnano.6b00021
ACS Nano XXXX, XXX, XXX−XXX