

Tunable Tribotronic Dual-Gate Logic Devices Based on 2D MoS₂ and Black Phosphorus

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With the Moore's law hitting the bottleneck of scaling-down in size (below 10 nm), personalized and multifunctional electronics with an integration of 2D materials and self-powering technology emerge as a new direction of scientific research. Here, a tunable tribotronic dual-gate logic device based on a MoS₂ field-effect transistor (FET), a black phosphorus FET and a sliding mode triboelectric nanogenerator (TENG) is reported. The triboelectric potential produced from the TENG can efficiently drive the transistors and logic devices without applying gate voltages. High performance tribotronic transistors are achieved with on/off ratio exceeding 106 and cutoff current below 1 pA μm^{-1} . Tunable electrical behaviors of the logic device are also realized, including tunable gains (improved to ≈ 13.8) and power consumptions (≈ 1 nW). This work offers an active, low-power-consuming, and universal approach to modulate semiconductor devices and logic circuits based on 2D materials with TENG, which can be used in microelectromechanical systems, human-machine interfacing, data processing and transmission.

these problems, the transistors based on 2D materials are intensively investigated, demonstrating improved gate control over the channel barrier and reduced short-channel effects due to the atomic thickness.^[5–8] Emerging 2D materials, such as transition metal dichalcogenides,^[9] black phosphorus (BP),^[10] and graphene,^[11] offer good options for ultimate thin channel transistors, and promise a bright future for the next generation of semiconductors.^[12,13] However, the fabrication of ultrashort channel and scaling integration with conventional micro-nanofabrication technologies, especially for sub-10 nm transistors, is still a challenge. Therefore, the IT technology is currently developing toward another direction, i.e. personalized, diverse, and soft electronics with the integration of multifunctional components and self-powering technology.^[14–17]

The Moore's law has directed the development of semiconductor industry since 1965, which predicts that the density of devices on a chip doubles every 18 months.^[1–4] Although researchers have pursued the scaling-down technology of field-effect transistor (FET) for high-speed CPU, short channel effect is pronounced in sub-10 nm scale. Direct source-to-drain tunneling and the loss of gate electrostatic control on the channel severely deteriorate the leakage current at off state, thus limiting the scaling down of Si transistors. To address

triboelectric nanogenerators (TENGs) that convert mechanical energy into electricity have been extensively developed.^[15,18–21] due to the great potential for driving self-powered personal electronics,^[22] active strain/force sensors,^[23] human-machine interface,^[24] and modulating semiconductor devices.^[25] By conjunction of triboelectrification and electrostatic induction, triboelectric potential produced by TENGs can work as a gate voltage to control/tune charge carriers transport in the channel of transistors, i.e. tribotronic transistor (or contact electrification

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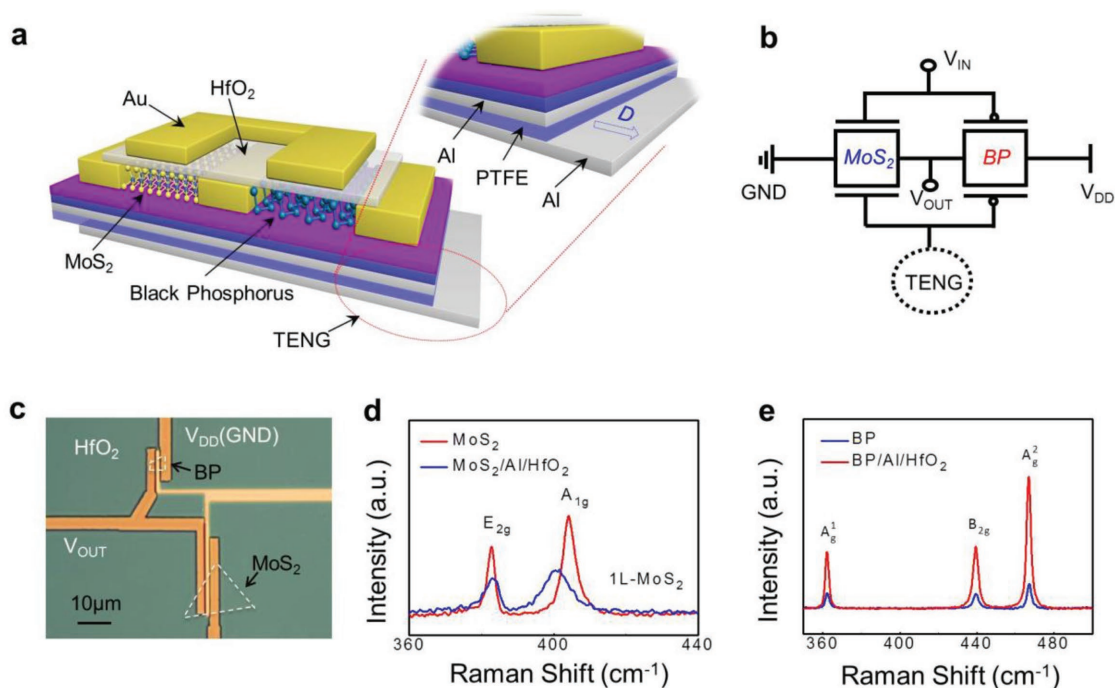


Figure 1. Schematic illustration and materials characterization. a) Schematic illustration of the tunable dual-gate tribotronic logic device composing of *n*-type MoS₂ and *p*-type BP FETs. b) Circuit diagram of the dual-gate tribotronic logic device. c) Optical image of the logic device. d) Raman spectra of pristine MoS₂ and MoS₂ with Al/HfO₂. e) Raman spectra of few-layer pristine BP and BP with Al/HfO₂.

field-effect transistor).^[26,27] In this case, triboelectric potential induced by external mechanical stimuli replaces the gate voltage input and greatly decreases the power consumption. The coupling between triboelectric potential and electrical behaviors in semiconductor materials achieves unprecedented device characteristics and leads to an emerging field of tribotronics, bridging various external mechanical stimuli and semiconducting behaviors, which represents a universal application in mechanical motion-triggered memory device,^[28] smart tactile switch,^[22,29] and tunable phototransistor.^[30,31] The logic circuits commonly implemented with transistors are the basic components in the integrated circuit and have a wide range of applications in computers, digital control circuits, communications, and instrumentation.^[32–38] Dual-gate FETs comprised of a bottom gate and an extra top gate are essential in logic circuits according to the facile and accurate modulation of threshold voltage (V_{th}) through the second gate, which electrostatically modifies the charge carrier transportation in the channel accumulated by the first gate.^[39–42]

Here, we report a tunable tribotronic dual-gate logic device based on *n*-type MoS₂ FET, *p*-type BP FET, and a sliding-mode TENG. Both types of transistors are connected to construct the logic device with SiO₂ as the bottom gate dielectric layer and HfO₂ as the top gate dielectric layer. Triboelectric potential produced from the sliding-mode TENG under external displacement can efficiently drive the transistors and logic devices through bottom SiO₂ dielectrics instead of applying gate voltages. The high- κ top gate dielectrics (HfO₂) contribute to the increase of the effective capacitance of the device, leading to high-performance tribotronic transistors with current on/off ratio exceeding 10⁶ and cutoff current below 1 pA μm^{-1} ,

which is the best ever obtained. When gate voltage is applied on the top gate, tunable electrical behaviors of the logic device are achieved according to different displacements of TENG coupled to the bottom gate, including tunable gain (improved to be ≈ 13.8) and static power consumption (reduced to be ≈ 1 nW). Besides, electrical performances of tribotronic MoS₂ FET and logic device are characterized in details in this work. Based on this, the figure-of-merits of tribotronic transistor and logic device involving tribotronic transconductance, tribotronic subthreshold swing (SS_1), and logic gate power consumption have been proposed for the first time. Coupling semiconductor devices with TENGs realizes the control of logic devices through external instructions, offering an active and low-power-consuming way for device operation. The tunable tribotronic device is believed to have great potential in human-machine interaction, electronic skin, intelligent sensor, and other wearable devices for necessary logic operation in active mode. The proposed figure-of-merits of tribotronic devices are also of great significance for the development of sophisticated semiconductor devices coupled with TENGs.

Figure 1a is the schematic illustration of the tunable tribotronic dual-gate logic device, and the optical photograph is shown in Figure 1c, which is composed of a dual-gate complementary inverter coupled with a TENG operated in lateral-sliding mode. MoS₂ and BP are used as the *n*-type and *p*-type channels in the complementary devices, respectively. Robust silicon wafer with 300 nm thermally grown SiO₂ is chosen as the substrate for facile coupling with TENG. High- κ HfO₂ is used as the top-gate dielectric for efficient modulation of carrier transportation in FET channels. To fabricate the tunable logic device, nano-flakes of MoS₂ were first grown on SiO₂/Si wafer by chemical

vapor deposition (CVD) (details in the Experimental Section). Few-layer (2–10 layers) BP flakes were then transferred onto the substrate by mechanical exfoliation. The Cr/Au source-drain electrodes (10 nm/30 nm) were defined by standard e-beam lithography (EBL) and electron-beam deposition. The HfO₂ top gate dielectric layer (30 nm) was grown through atomic layer deposition (ALD), with subsequent top gate electrodes deposition by EBL and metallization. Before coupling with the TENG, an aluminum layer was deposited on the bottom of the silicon substrate for excellent ohmic contact. Meanwhile, it served as one electrode of the TENGs, under which a polytetrafluoroethylene (PTFE) layer was attached as one of the triboelectrification layers. Another aluminum tape attached onto a mobile acrylic board was selected as the other triboelectrification layer. Triboelectric potential could be induced through triboelectrification and electrostatic induction during lateral sliding of the mobile acrylic board and functionalized as a voltage input through bottom gate. The circuit diagram of the tribotronic dual-gate logic device is shown in Figure 1b. Both types of the transistors are connected to construct the logic device with SiO₂ as the bottom gate dielectric layer and HfO₂ as the top gate dielectric layer. Here, the top gate with high- κ dielectric is a necessary assistant for efficient modulation of carrier concentration in the tribotronic FET, which will be discussed below in details.

The optical photograph of the as-synthesized monolayer MoS₂ flakes is shown in Figure S1b in the Supporting Information, with a thickness of 0.7 nm confirmed by atomic force microscope. Few-layer (2–10 layers) BP flakes were mechanically exfoliated from bulk crystal, with a thickness of around 4 nm (the optical photograph is shown in Figure S1c in the Supporting Information). The Raman spectra of pristine MoS₂ and MoS₂ encapsulated with Al/HfO₂ were excited using 532 nm laser, as shown in Figure 1d. The peak of out-of-plane A_{1g} vibration modes shows a red-shift from 404.1 to 401.6 cm⁻¹ as MoS₂ is encapsulated with Al/HfO₂, while the peak of in-plane E_{2g} vibration modes remains at 382.7 cm⁻¹. The full widths at half maximum of the A_{1g} and E_{2g} vibration modes increase by ≈ 5 cm⁻¹ and ≈ 1.2 cm⁻¹, respectively. The wavenumber difference between E_{2g} and A_{1g} vibration modes decreases from 21.4 to 17.9 cm⁻¹. It has been reported that the phonon of A_{1g} vibration modes couple with electrons more strongly compared with the phonon of E_{2g} vibration modes. The softening and broadening A_{1g} peak of MoS₂ encapsulated with HfO₂ may be attributed to the electrons doping of the monolayer MoS₂ during the Al/HfO₂ deposition, while the E_{2g} vibration modes is weakly dependent on the doping.^[43] The predeposition of 1 nm Al at the MoS₂/HfO₂ interface imposes an additional coulomb scattering and roughness scattering, which interacts strongly with the out-of-plane A_{1g} vibration modes, resulting in the increase of the carrier scattering.^[43–46] For the Raman spectra of BP, no distinct differences of Raman peaks are observed between pristine few-layer BP and HfO₂ encapsulated few-layer BP (Figure 1e), indicating the encapsulation of high- κ HfO₂ has less effect on BP flakes compared with MoS₂. All the characteristic peaks (A_g¹, B_g², and A_g²) are clearly visible at the wave numbers of 362 cm⁻¹, 439 cm⁻¹, and 467 cm⁻¹, respectively.^[33] Photoluminescence spectra of pristine monolayers MoS₂ and Al/HfO₂ encapsulated MoS₂ are shown in Figure S1a in the Supporting Information. The

pristine monolayer MoS₂ displays a strong PL peak at 1.82 eV, originating from its bandgap. However, the PL peak at 1.82 eV is quenched after Al/HfO₂ encapsulation. There is a weak peak at 1.77 eV related with impurities, which may be attributed to the predeposition of 1 nm Al seeding layer before HfO₂ ALD process.

As shown in Figure 2a, dual-gate MoS₂ FET is integrated with a sliding mode TENG, which is essentially a single electrode mode nanogenerator with top PTFE friction layer and grounded Al friction electrode. When both friction layers contacted with each other at the initial state, the bottom surface of the PTFE layer showed negative charges and attracted positive charges on the top surface of the Al layer according to their different triboelectric polarities. The negative and positive charges were balanced, demonstrating no potential applied to the gate electrode (equivalent to zero gate voltage input). We defined the relative displacement in horizontal between the PTFE layer and the mobile Al layer direction with parameter D , as marked in the figures. As the mobile aluminum layer was horizontally slid to right side at a certain displacement (D), the positive charges on the nonoverlapped aluminum electrode flowed to ground. Meanwhile, the negative charges left on the PTFE layer induced a negative triboelectric potential, functionalized as a negative gate voltage input. With the displacement increased, the negative triboelectric potential tended to be enhanced. The operation mechanism of MoS₂ tribotronic device can be explained in terms of the band diagrams, as show in Figure 2b. The negative triboelectric potential originated from the displacement depleted more free electrons in MoS₂ channel, which would raise the Schottky barrier height ϕ_b at interface between source electrode and the semiconductor MoS₂. And the increasing of the Schottky barrier ϕ_b gradually decreased the drain current. Therefore, the n -type tribotronic transistors work in depletion mode.^[25] Figure 2c shows the typical output characteristics of n -type MoS₂ FET through bottom gating. When the gate voltage (V_G) decreased from 0 to -15 V, the drain current (I_D) gradually decreased from 0.23 to 0.33 pA at a drain voltage (V_D) of 3 V, demonstrating a high on-current density of 29 $\mu\text{A } \mu\text{m}^{-1}$ and low off-current density of 0.04 pA μm^{-1} . The inset of Figure 2d shows the optical image of MoS₂ FET with channel length at 2 μm and channel width at 8 μm . The corresponding transfer characteristic of the fabricated device ($V_D = 0.1$ V) is shown in Figure 2d, exhibiting ultra-high current on/off ratio of $\approx 10^9$ and low SS of 180.6 mV/dec. The field effect mobility extracted from the transfer curve is ≈ 21.6 cm²·V⁻¹·s⁻¹. Moreover, top gate contributes to the enhanced modulation ability of the bottom gate or TENG due to the capacitance coupling of top gate and bottom gate dielectrics.^[34,35] The effective capacitance (C_{eff}) of the dual-gate FET was defined as $C_{\text{eff}} = C_{\text{BG}} + (C_{\text{TG}}^{-1} + C_{\text{BT}}^{-1})^{-1}$, in which C_{TG} was the top gate capacitance, C_{BG} was the back gate capacitance, and C_{BT} was the coupling capacitance. As $C_{\text{BT}} \gg C_{\text{TG}} \gg C_{\text{BG}}$, the effective capacitance was approximately equal to the top gate capacitance according to the aforementioned equation.^[9,49] Therefore, even gating through the bottom SiO₂ gate dielectrics, top gate played an assistant role in the modulation of MoS₂ channel due to the capacitance coupling effect. Detailed discussions of the capacitance coupling

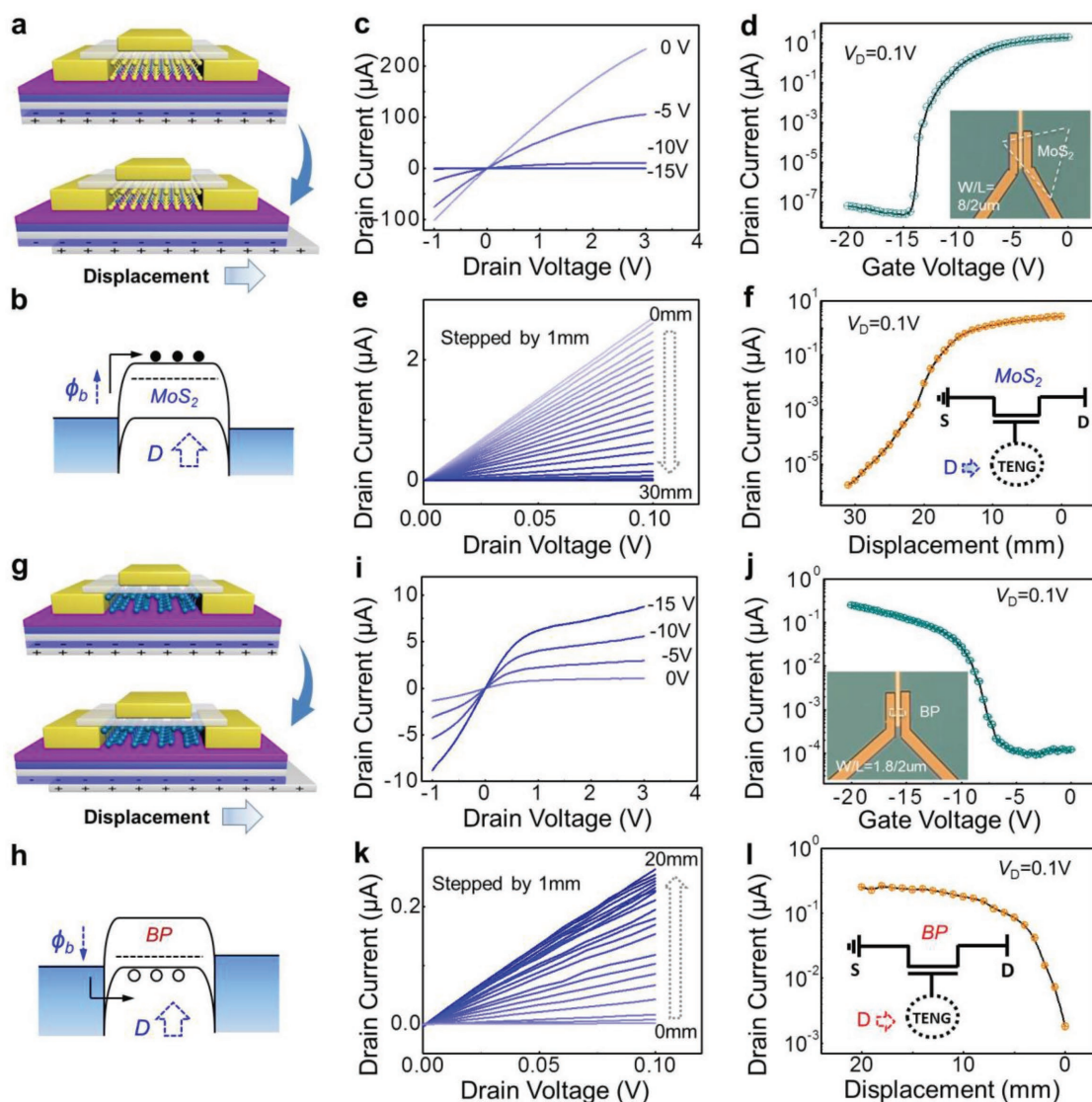


Figure 2. Electrical performance of top-gate-assisted MoS₂ and BP tribotronic transistors. a) Schematic illustration of the working principle of tribotronic MoS₂ transistor. b) The energy band diagram of the tribotronic MoS₂ transistor at a certain displacement. c) and d) Typical output performance and transfer curve of the MoS₂ transistor, and the inset is the optical photograph of the device. e) and f) Output performance and transfer characteristics of the tribotronic MoS₂ transistor, the inset is the circuit diagram. g) Schematic illustration of the working principle of tribotronic BP transistor. h) The energy band diagram of tribotronic BP transistor at a certain displacement. i) and j) Typical output characteristics and corresponding transfer characteristics of the BP FET, and the inset is the optical photograph of the device. k) and l) Typical output characteristics and transfer characteristics of the tribotronic BP transistor, the inset is the corresponding circuit schematic.

effect are shown in supporting information and Figure S2. Interestingly, the modulation of MoS₂ channel with top gate grounding is sharply degraded, as shown in Figure S2a in the Supporting Information, which is attributed to the screening effect of the grounded top gate.

According to the assistant function of top gate, high performance of tribotronic MoS₂ FET was also achieved. The displacement of Al friction electrode beard on acrylic board was kept in horizontal direction through a custom linear motor controller, which efficiently eliminated the electrostatic interference from manual operation. The relationship between triboelectric potential V_{TENG} and displacement of TENGs was first characterized, as shown in Figure S3a in the Supporting Information.

V_{TENG} shows a linear relationship with displacement D , which

is defined by $V_{TENG} = \frac{\sigma}{C_d} \approx \frac{-kD}{C_d}$, where σ is the induced charge

density, C_d is the specific capacitance of dielectric layer, and k is a proportional constant. According to the assistant function of top gate, high performance of tribotronic MoS₂ FET was also achieved. The displacement of Al friction electrode beard on acrylic board was kept in horizontal direction through a custom linear motor controller, which efficiently eliminated the electrostatic interference from manual operation. Output performance of tribotronic MoS₂ FET is shown in Figure 2e. With Al friction electrode marching 30 mm to the right direction

(stepped by 1 mm), I_{DS} decreased. The output curves of the tribotronic transistors were all linear, indicating excellent Ohmic contact formed between MoS₂ and Au source-drain electrode. Figure 2f shows the corresponding transfer characteristics of the tribotronic transistors, extracted from Figure 2e. I_D decreased from 2.7 to 1.68 pA, with displacement of Al friction electrode from 0 to 30 mm at $V_D = 0.1$ V. Under the variation range of the displacement, the current on/off ratio reached as high as $\approx 10^6$ with off-current at pA level, which was very important for the application of logic devices. The inset is the circuit diagram of the MoS₂ transistor coupled with TENG. The tribotronic transfer characteristics were comparable with that of back gate FET in Figure 2d, indicating our triboelectric potential supplied by TENGs can completely replace the gate voltage, realizing active modulation of charge carriers in FET channel. In order to present the tribotronic output performance and transfer characteristics of the MoS₂ tribotronic transistors more precisely, a larger range sweep date was added in Figure S8a–b in the Supporting Information, with the drain voltage swept from -0.1 to 1 V. This device performance displaced a relatively small threshold voltage and larger on-off ratio, which can reach as high as 5×10^7 with $V_D = 0.1$ V, and the drain current can be cut off below 0.5 pA when $D = 14$ mm. For larger drain voltage of 1 V, the cutoff current increased to 0.18 nA, but still maintained a larger on-off ratio of 1.1×10^6 .

Notably, the static triboelectric potential can maintain the channel current at a stable value due to the low leakage current and excellent insulating properties of both top and back gate dielectrics. Real-time characterization of output currents under different displacements is demonstrated in Figure S3b in the Supporting Information. When the displacement changed from 0 to 20 mm stepped with 1 mm, the current showed a stepped decrement and dropped below to ≈ 0.2 nA when D was >14 mm. Periodic dynamic measurement was performed as shown in Figure S3c in the Supporting Information, with displacement D changed between 0 and 20 mm in a period at 2 s. Over 100 s of external displacements, the current on/off ratio was stable and maintained to be over 10^4 .

We took MoS₂ tribotronic transistors as an example to illustrate the figure-of-merits of tribotronic transistors in details. We introduced the concept of tribotronic transconductance (g_t) and SS_t for the first time. The g_t characterized the tribotronic electric control ability of the linear sliding TENGs. The SS_t was defined as the variation of displacement required for one order of magnitude change in drain current, indicating the switching speed of tribotronic transistors at subthreshold region. The figure-of-merits of the tribotronic transistors were discussed in details in supporting information (Figure S3, Supporting Information).

Similar with tribotronic MoS₂ FET, tribotronic BP FET was also coupled with a sliding mode TENG (Figure 2g). The operation mechanism of BP tribotronic device can be explained in terms of the band diagrams, as show in Figure 2h. The negative triboelectric potential induced by displacement accumulated the holes (majority carrier) in the p -type BP conduction channel and created an enhancement zone, which will reduce the Schottky barrier height ϕ_b at interface between source electrode and the semiconductor BP. And the decreasing of the

Schottky barrier ϕ_b gradually increased the corresponding drain current. Therefore, the p -type tribotronic transistors worked in enhancement mode. Figure 2i shows typical output characteristics of p -type BP FET through bottom gating, indicating a drain current saturation trend at $V_D > 1$ V. Figure 2j shows the corresponding transfer characteristics of the fabricated device, representing a V_{th} at -7 V and current on/off ratio over 10^3 at $V_D = 0.1$ V. The inset is the optical image of BP FET, with channel length at $2 \mu\text{m}$ and channel width at $1.8 \mu\text{m}$. I_D of the fabricated BP transistor is smaller than 10^{-6} A at a gate voltage of -30 V, which may be attributed to surface oxidation of BP channel during the fabrication process. Especially during the ALD process of HfO₂, the water vapor in the chamber may deteriorate the electrical performance of BP nanoflakes. Electrical performance of tribotronic BP FET was also characterized with the assistant of linear motor controller. We controlled the linear motor to march from 0 to 20 mm, stepped by 1 mm. The output drain currents were measured simultaneously at each step, with drain voltage sweeping from 0 to 0.1 V (Figure 2k). The data in Figure 2l is the corresponding transfer characteristics of the tribotronic transistors (extracted from Figure 2k), showing an obvious p -type properties of transistors. The current on/off ratio was $\approx 10^3$, with drain voltage at 0.1 V. The inset is the circuit diagram of the tribotronic BP FET. The transfer characteristics of tribotronic p -type FET were comparable with that of pristine BP FET shown in Figure 2j, indicating the triboelectric potential supplied by TENGs could also efficiently drive p -type FETs. In order to present the tribotronic output performance and transfer characteristics of the BP tribotronic transistors more precisely, a larger range sweep date was added in Figure S8(c–d) in the Supporting Information, with the drain voltage swept from -1 to 3 V. For larger drain voltage of -1 V, the on-off ratio is $\approx 10^2$.

After achieving stable properties of MoS₂ and BP tribotronic FETs, tribotronic logic device coupled with TENG was characterized, gating through bottom SiO₂ dielectrics. As shown in Figure 3a, the tribotronic logic device is composed of a dual-gate inverter based on complementary 2D materials on Si/SiO₂ substrate with Au/HfO₂ top gate, and a linear sliding TENG with the structure of Al-PTFE-Al. The circuit diagram is shown in the bottom panel of Figure 3a. In this structure, top gate played an assistant role for capacitance coupling without applying top gate voltage. Figure 3c shows a typical voltage transfer characteristics of the inverter based on complementary 2D materials, and the inset shows the corresponding circuit schematic diagram, with MoS₂ channel connected to the source electrode. To yield the same resistance value for the n-channel and p-channel of the circuit, our logic inverter displayed the inversion point at -15 V, along with a logic separation of 0.99 V. The voltage gain is ≈ 2 at a small V_{DD} of 1 V (The voltage gain can reach as high as 4.8 at $V_{DD} = 2$ V, as shown in Figure S4 in the Supporting Information). The working principle of the tribotronic logic device is shown in Figure 3b. In the initial state (PTFE and Al friction layers were fully contacted, equivalent to an input voltage at 0), n -type MoS₂ tribotronic transistor (connected to the ground) worked in low-resistance state, while BP tribotronic transistor worked in high-resistance state. To yield the same resistance value between MoS₂ and BP channel, the output voltage was pulled down to 0 V (defined as low

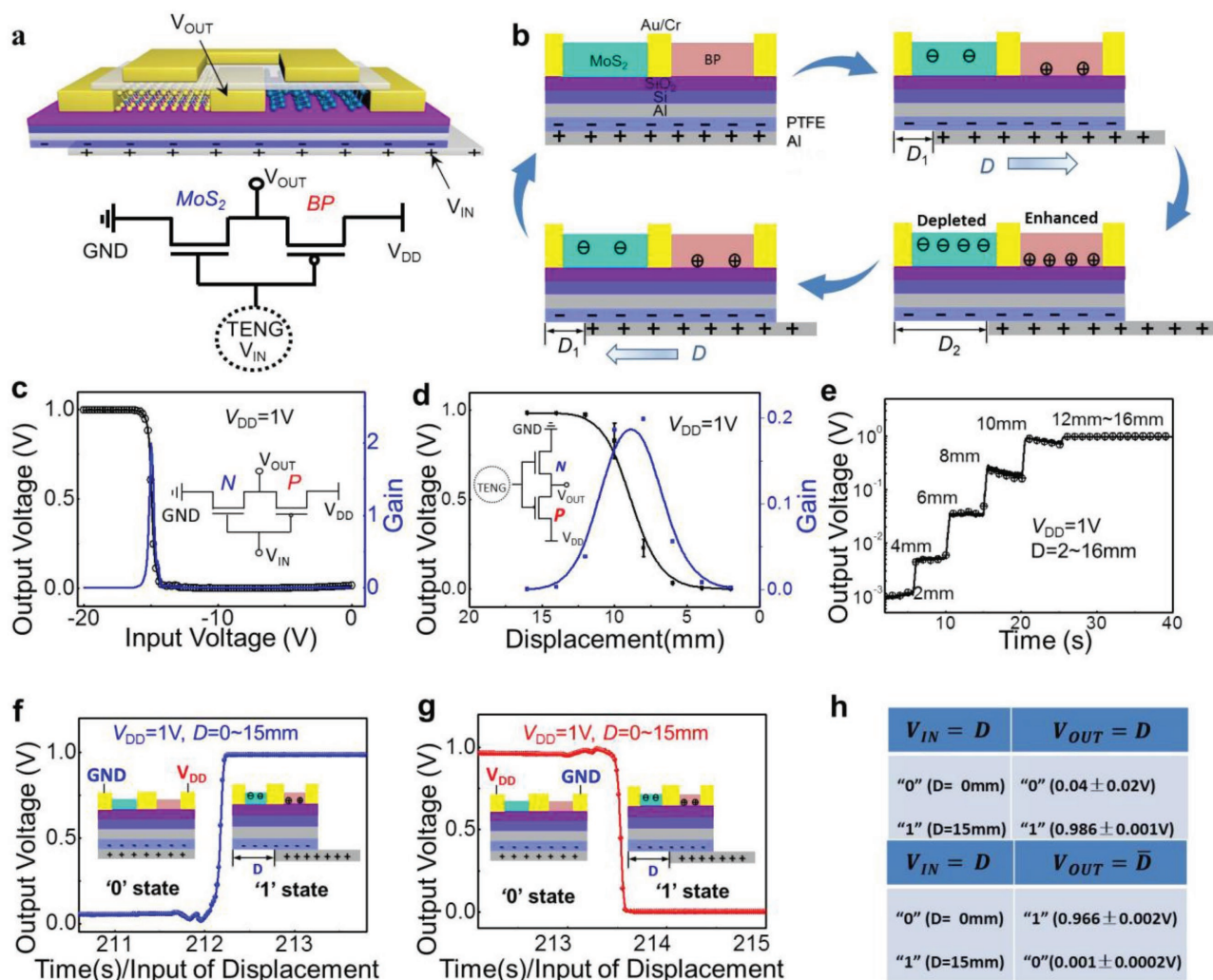


Figure 3. Electrical performance of tribotronic logic inverter based on n-MoS₂ and p-BP. a) Schematic illustration of tribotronic logic inverter and its circuit schematic diagram. b) The working principle of the tribotronic logic device. c) Voltage transfer characteristic and the corresponding gain of the complementary inverter based on MoS₂ and BP FETs, the inset is the corresponding circuit diagram. d) Voltage transfer characteristic and the corresponding tribotronic gain of the tribotronic logic inverter, inset shows its circuit diagram. e) Output voltage of the tribotronic logic device under different displacements, from 0 to ≈16 mm stepped by 2 mm. f) Match gate of tribotronic logic device, with MoS₂ FET grounding, the inset shows the corresponding schematic diagram, $D=0$ and $D=15$ was defined as "0" state and "1" state, respectively. g) NOT gate of tribotronic logic device, with BP FET grounding, the inset shows the corresponding schematic diagram. h) Truth table of match gate and NOT gate.

level/"0" state). When the bottom Al electrode slid to a certain displacement (D_1), the TENG produced a negative triboelectric potential, which depleted electrons and accumulated holes in MoS₂ and BP channel, respectively. Therefore, the output voltage was increased. With the displacement (D_1) increasing to the maximum value (D_2), the electrons in MoS₂ channel were further depleted and holes were further accumulated in BP channel. The output voltage was pulled up to the supplied voltage (V_{DD}). When the bottom Al electrode began to slide back to the initial position, the negative triboelectric potential gradually diminished and the output voltage recovered to the initial value (0). Figure 3d shows the voltage transfer characteristics of the tribotronic logic inverter, consistent with the working principle discussed above. The extracted tribotronic gain was ≈0.2 V mm⁻¹. Figure 3e shows the dynamic testing of

tribotronic inverter logic device. With the displacement changing from 2 to 16 mm stepped by 2 mm, the output voltage increased from 0.001 to 0.986 V. When the displacement is larger than 12 mm, the output voltage of the tribotronic inverter reached a stable high level. Supposing the initial position ($D=0$ mm) of TENGs was the '0' state, the separation position ($D=15$ mm) was the "1" state. When the MoS₂ FET was grounded, the output voltage of tribotronic logic inverter changed from low level ($V_{OUT}=0$) to high level ($V_{OUT}=1$ V) with TENG changing from "0" state to "1" state, i.e. a match gate (Figure 3f). When BP FET was grounded, the output voltage of tribotronic logic inverter changed from low level ($V_{OUT}=1$ V) to high level ($V_{OUT}=0$) with TENG changing from "0" state to "1" state, i.e. a NOT gate (Figure 3g). The corresponding truth table of match gate and NOT gate is shown in Figure 3h. Dynamic cycle stability

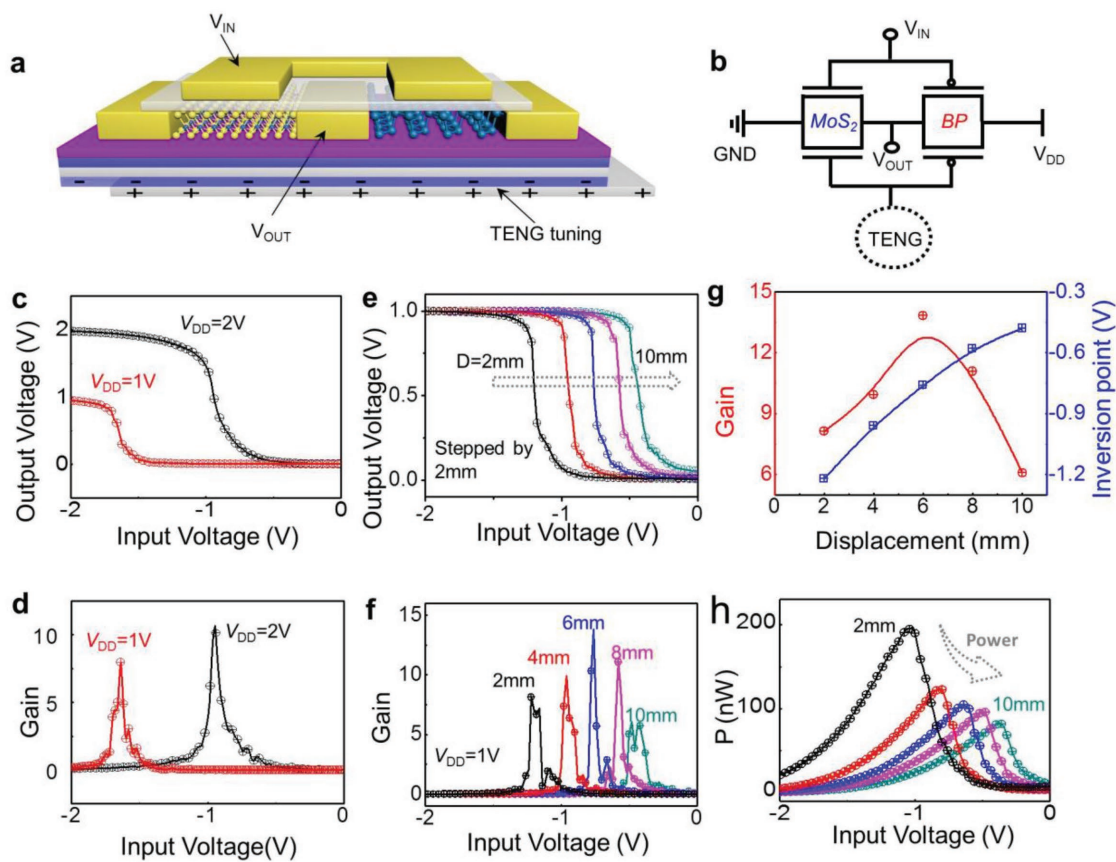


Figure 4. Electrical performance of TENGs modulated top gate inverter. a) Schematic illustration and b) circuit diagram of tunable dual-gate tribotronic inverter. c) Typical voltage transfer characteristics of top gate inverter with $V_{DD} = 1$ and 2 V, respectively, and d) the corresponding voltage gains. f) Voltage transfer characteristic of TENGs modulated inverter, with displacement changing from 2 to 10 mm stepped by 2 mm. g) Summarization of the modulated gains and inversion points vs. displacements. h) Modulated power consumption according to different displacements.

tests were also conducted for both match gate and NOT gate. Over 100 cycles of external displacements, the logic separation could be maintained well (Figure S5, Supporting Information).

To demonstrate the tunable properties of the tribotronic dual-gate logic device, top gate voltage was applied to drive the complementary inverter and TENG was coupled with bottom gate. The schematic illustration of TENGs modulated inverter is shown in Figure 4a, and its circuit diagram is shown in Figure 4b. Input voltage was applied through top HfO_2 gate dielectric layer for low voltage operation, while the sliding mode TENG was coupled with the bottom Si wafer according to the robust friction durability. Typical voltage transfer characteristics of the complementary inverters with voltage inputs through top gate were obtained under two supplied voltages ($V_{DD} = 1$ and 2 V, Figure 4c). The corresponding voltage gains are 8 and ≈ 10 , respectively (Figure 4d), which is comparable with the inverter using BP and MoS_2 transistors reported before.^[50] Voltage transfer curves of the inverter modulated by TENG were subsequently characterized. With displacement D of the mobile Al electrode changing from 2 to 10 mm stepped by 2 mm, the inversion points shifted from -1.2 to -0.4 V according to the voltage transfer characteristics (Figure 4e). The corresponding voltage gains were also tunable as shown in Figure 4f. The maximum gain value could reach 13.8 at a

displacement of 6 mm with TENG, which was $\approx 74\%$ higher than the original value (≈ 8 , without TENG modulation). The supply voltage V_{DD} was 1 V in all the cases. The variations of inversion point and voltage gain with the displacement of TENG were summarized in Figure 4g. To explore the mechanism of tunable properties of tribotronic dual-gate logic device, corresponding tunable electrical properties of dual gate MoS_2 and BP transistors were investigated (Figure S6, Supporting Information). Different displacements induced different triboelectric potentials coupling to FETs and modulated charge carriers density in transistor channels. Therefore, the linear sliding mode TENG gating through the back gate could modulate the V_{th} of both MoS_2 and BP FETs to realize the shift of inversion points. Meanwhile, the voltage gain could be modulated and enhanced through matching the conductivity and V_{th} of MoS_2 and BP transistors with TENG at different displacements.

In conclusion, to achieve an active and low-power consuming way to logic devices, a sliding mode TENG was coupled with a dual-gate complementary inverter based on n -type MoS_2 and p -type BP FETs for the first time. The triboelectric potential of TENG induced by triboelectrification and electrostatic induction can replace the gate voltages and modulate the carrier's transportation in complementary inverter with MoS_2

and BP as the *n*-type and *p*-type channels, respectively. The tribotronic MoS₂ FET and BP FET worked in depletion mode and enhancement mode, respectively. Based on this, a tribotronic complementary inverter was achieved with triboelectric potential as the input voltage. Both the tribotronic FETs and inverters represented low voltage operation and low energy consumption due to the substitution of gate voltage inputs with the output voltages from TENGs. Furthermore, with an extra top gate structure, the displacement of TENG was able to tune the electrical properties of FETs and inverter, including the threshold voltages, inversion points, gain values and static power consumption. Notably, the displacements of sliding mode TENG are equivalent to the separation distances of contact-separation mode or single electrode mode TENG, all of which associate with external mechanical instructions (or operations). The tribotronic systems coupling TENG and semiconductor devices promise a universal and direct way to human-machine interface, intelligent sensing, wearable devices and electronic skin. This work reported the fundamental dual-gate tribotronic complementary inverter. More complicated tribotronic logic circuits (such as AND, OR, NAND, NOR, ring oscillators, and even microprocessor) based on 2D materials are demanded to be developed for advanced functions. Compact integration of TENGs and semiconductor devices is significant for tribotronic integrated circuit. Particular correspondences are also critical to be unified between complex human actions and electric signals. With the rapid development of self-powered systems and large area 2D materials growth technology, the proposed tunable tribotronic logic devices will contribute to the development of sophisticated logic circuits for active data processing and transmission in micro-electromechanical systems and human-robot interfacing.

Experimental Section

Materials Preparation: First, MoS₂ was grown on an Si wafer (with 300 nm thermally grown SiO₂) by CVD at 850 °C. MoO₃ power and sulfur pieces were used as the precursors. The MoO₃ power in the quartz tube was heated to 850 °C with a rate of 30 °C min⁻¹. And the sulfur pieces were heated to 150 °C at the same time. During the growth process, the flow rate of argon was maintained at 50 sccm to provide an inert atmosphere and carry the vapor of the precursors. The pressure in the quartz tube was kept at 1 kPa. The tube was quickly cooled down to room temperature after the growth process of MoS₂. Few-layer (2–10 layers) BP flakes were mechanically exfoliated from bulk crystal using a scotch tape and then transferred onto the Si wafer with grown MoS₂.

Device Fabrication: After the preparation of MoS₂ and BP on the Si wafer, the source/drain electrodes were subsequently defined by standard EBL and electron-beam evaporation of Cr/Au (10/30 nm, respectively). Then, top dielectric layer (HfO₂, 30 nm) was processed using ALD (PICOSUN/SUNALE R-200). Finally, top gate electrodes were defined by EBL. Next the TENGs coupled with the logic inverter above were prepared. An aluminum layer was deposited on the bottom of the silicon wafer for Ohmic contact, under which a PTFE layer was attached and selected as one triboelectrification layer. A mobile aluminum tape attached on an acrylic substrate was used as the other triboelectrification layer and located to fully contact with PTFE layer. The mobile aluminum friction layer could be horizontally slid by an external force and induced the triboelectric potential as the voltage input for FET and inverter.

Performance Characterization: The Raman and PL characteristics were measured by a HORIBA/LabRAM HR Evolution spectrograph. The wavelength of the excitation laser was 532 nm. The electrical characterization of the tribotronic transistors and tribotronic logic device was conducted with a semiconductor parameter analyzer (Agilent B1500A) in a probe station under ambient environment. The displacements of TENGs were controlled by a linear motor. The output of TENGs was characterized by Keithley 6514 system electrometer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D materials, triboelectric nanogenerators, tribotronic logic inverters, tribotronic transistors

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