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MoS_2 Negative-Capacitance Field-Effect Transistors with Subthreshold Swing below the Physics Limit

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The Boltzmann distribution of electrons induced fundamental barrier prevents subthreshold swing (SS) from less than 60 mV dec^{-1} at room temperature, leading to high energy consumption of MOSFETs. Herein, it is demonstrated that an aggressive introduction of the negative capacitance (NC) effect of ferroelectrics can decisively break the fundamental limit governed by the "Boltzmann tyranny". Such MoS_2 negative-capacitance field-effect transistors (NC-FETs) with self-aligned top-gated geometry demonstrated here pull down the SS value to 42.5 mV dec^{-1}, and simultaneously achieve superior performance of a transconductance of 45.5 µS µm and an on/off ratio of 4×10^6 with channel length less than 100 nm. Furthermore, the inserted HfO_2 layer not only realizes a stable NC gate stack structure, but also prevents the ferroelectric P(VDF-TrFE) from fatigue with robust stability. Notably, the fabricated MoS_2 NC-FETs are distinctly different from traditional MOSFETs. The on-state current increases as the temperature decreases even down to 20 K, and the SS values exhibit nonlinear dependence with temperature due to the implementation of the ferroelectric gate stack. The NC-FETs enable fundamental applications through overcoming the Boltzmann limit in nanoelectronics and open up an avenue to low-power transistors needed for many exciting long-endurance portable consumer products.

With the miniaturization of silicon based metal-oxide-semiconductor field-effect transistors (MOSFETs) and their high-density integration on a chip, short-channel effects (SCEs) induced high system power dissipation is becoming a challenge for low-power applications.[1,2] The scaling down of MOSFETs' feature size involves SCEs and increased gate leakage current that gives rise to the bottlenecks in miniaturization: degraded on/off characteristics and heat generation during each switching event, leading to excessive power dissipation, horrible device reliability, and high leakage current.[3,4] Thus, such nonideal effects hinder the MOSFETs to maintain high performance at short channel length (L_{ch}), deviating from Moore's Law. Therefore, reducing threshold voltage (V_{th}) and subthreshold swing (SS) are essential for realizing low-power dissipation per switching event.[2,5,6]

The theoretical characteristic length (λ) of short-channel MOSFETs with planar geometry can be calculated as $\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}}$,

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in which ε_s and ε_{ox} are dielectric constants of the semiconductor and gate insulator, t_s and t_{ox} are the thicknesses of channel layer and dielectric layer, respectively. So ultrathin property of both the dielectric layer and channel materials are required to reduce λ, and that is also the motivation for continuously pursuing low equivalent oxide thickness (EOT) with high-k dielectrics and exploring new channel materials. Transition metal dichalcogenides (TMDs) layered materials have been extensively studied for their high carrier mobility and ultrathin body characteristics, are of great interest for reducing operation voltage and achieving a high drive current. In particular, MOSFETs with MoS_2 as the active channel substantially presents immunity of SCEs compared to traditional bulk semiconductors, such as Si, Ge, and III-V compound materials.[7] However, once the L_{ch} is scaled down to sub 100 nm regime, the SCEs will degrade the performance of MoS_2 transistors.[8,9] Moreover, the Boltzmann limitation of SS ≥ 60 mV dec^{-1} at room temperature significantly impedes the ongoing scaling down of transistors.[10,11] The continued scaling of feature size eventually generates the realm of exploring new operation mechanisms for low-power applications. Such as impact ionization (I-MOS) FETs and tunnel FETs have been proposed to overcome the limitation, but both are required to change the transport mechanisms of carriers.[3,12] On the other hand, ferroelectric materials can be regarded as one kind of high-k dielectrics with spontaneous polarization, and an EOT value of about 1.1 nm can be achieved in a ferroelectric field-effect transistor (FeFET) by using ultrahigh-k gate dielectric $Pb(Zr_{0.52}Ti_{0.48})O_3$.[13] The negative-capacitance (NC) effect in such ferroelectrics is thought to be originated from the "S-shape" P–E curve, which is induced by highly nonlinearly in the polarization versus electric field (P–E) characteristics.[14] And the NC region (negative dP/dE regime) can be stabilized in series with a normal capacitor. NC field-effect transistors (NC-FETs) with ferroelectric gate stack is proposed to implement a step-up voltage transformer that will amplify the gate voltage thus leading to values of SS lower than 60 mV dec^{-1} and enabling low voltage operation.[15–17]

For initial verification, these studies have focused on the Si-based NC-FETs. The improved subthreshold behavior is achieved by electrostatically amplifying the channel surface potential, rather than introducing impact ionization and band-to-band tunneling mechanisms.[18,19]

Recently, MoS_2 NC-FETs with long gate length (L_{ch} > 100 nm) have been preliminarily demonstrated, and steep slope characteristics with SS below 60 mV dec^{-1} have been observed over a small range of channel current.[20–23] However, all those works employed the back-gated structures or internal metal gate (IMG) stack, so it is impossible to integrate multiple devices on the same chip with independent operation. Moreover, the electrostatic potential of floating IMG is unfixed and it will be affected easily by the nearby devices via coupling capacitances, which is undesired for practical digital applications. Until now, the operation principle of short-channel top-gated MoS_2 NC-FETs has not been fully clarified, so that systematical investigations are highly demanded, involving not only physical scalability, fabrication technologies, and temperature dependence, but also device reproducibility and reliability.

Herein, we present self-aligned top-gated MoS_2 NC-FETs with L_{ch} less than 100 nm by introducing a layer of ferroelectric poly(vinylidene fluoride-*co*-trifluoroethylene) (P(VDF-TrFE)) in the gate dielectric stack. It is shown that the thermionic bottleneck is broken in these devices with minimum SS value down to 42.5 mV dec^{-1} at room temperature. At first, the short channel (L_{ch} = 80 nm) MoS_2 NC-FETs with 30 nm thick P(VDF-TrFE) film are fabricated, and a high transconductance (g_m) of 45.5 μS μm^{-1}, a low V_{th} around −0.9 V and a high on/off ratio of >10^6 are simultaneously obtained. Furthermore, HfO_2 dielectric with optimized thickness is inserted to the top and bottom interfaces of the P(VDF-TrFE) layer for a stable negative-capacitance structure. In this case, the asymmetrical charge screening effect is reduced as well, resulting in robust reliability and stability of MoS_2 NC-FETs.[24] The electrical characteristic of NC-FETs with 4 nm HfO_2 and 26 nm P(VDF-TrFE) gate stack has been measured from 360 K down to 20 K, it is demonstrated that an ultrasmall SS value of 28.6 mV dec^{-1} and a high I_{on} of 131.25 μA μm^{-1} with V_{ds} of 0.5 V are obtained, and all these results matched the simulated results as well. Moreover, the obtained performance surpasses some of the best reported values, and the fabrication processes are also compatible with standard microfabrication technology.

Figure 1a–c gives a schematic comparison among a typical back-gated MoS_2 transistor, a short channel top-gated MoS_2 transistor and a top-gated MoS_2 NC-FET. Mechanical exfoliation is employed to fabricate MoS_2 flakes onto 300 nm SiO_2 coated Si substrates. Since monolayer MoS_2 transistors typically exhibit low carrier mobility and high contact resistance, few-layer (2–5 layers) MoS_2 flakes are utilized as the channel layer, as shown in Figure 1a.[25] Ag nanowires (NWs) (Figure S1 in the Supporting Information) are used as a "shadow mask" to fabricate the short-channel top-gated transistor, as shown in Figure 1b. And for a NC-FETs fabrication, a ferroelectric P(VDF-TrFE) layer is introduced to fill up the gap between the Ag NW top electrode and the bottom MoS_2 channel layer as shown in Figure 1c. Figure 1d gives a brief introduction of the fabrication processes of a MoS_2 NC-FET. First, Ag NWs are suspended by embedding them into the e-beam lithography photoresist with specific distance from the bottom MoS_2 channel layer, as shown in Figure 1d(I). After the source, drain, and gate electrodes are defined by e-beam lithography and metallization (Figure 1d(II)), 8 nm Au is deposited by e-beam evaporation with Ag NWs as a "shadow mask," forming a short channel transistor (Figure 1d(III)).[26,27] Then HfO_2 dielectric layer is fabricated via atomic layer deposition (ALD) approach, which can prevent ferroelectric P(VDF-TrFE) from fatigue and maintain a stable NC structure for operation reliability and stability (Figure 1d(IV)). Finally, followed by solution assembled ferroelectric P(VDF-TrFE) layer, a typical NC-FET is built (Figure 1d(V)).[28,29] And the electrical properties of the P(VDF-TrFE) thin film employed here are shown in Figure S2 in the Supporting Information).

Figure 2a shows an SEM image of a back-gated MoS_2 transistor (L_{ch} = 2 μm) with an Ag NW suspending over the MoS_2. Figure 2b is a typical transfer curves of a MoS_2 back-gated transistor with a 300 nm SiO_2 dielectric layer. The devices exhibit a mobility of 109.0 cm^2 V^{-1} s^{-1} and an on/off current ratio of ≈10^6, and no obvious SCEs are observed because the L_{ch} (2 μm)

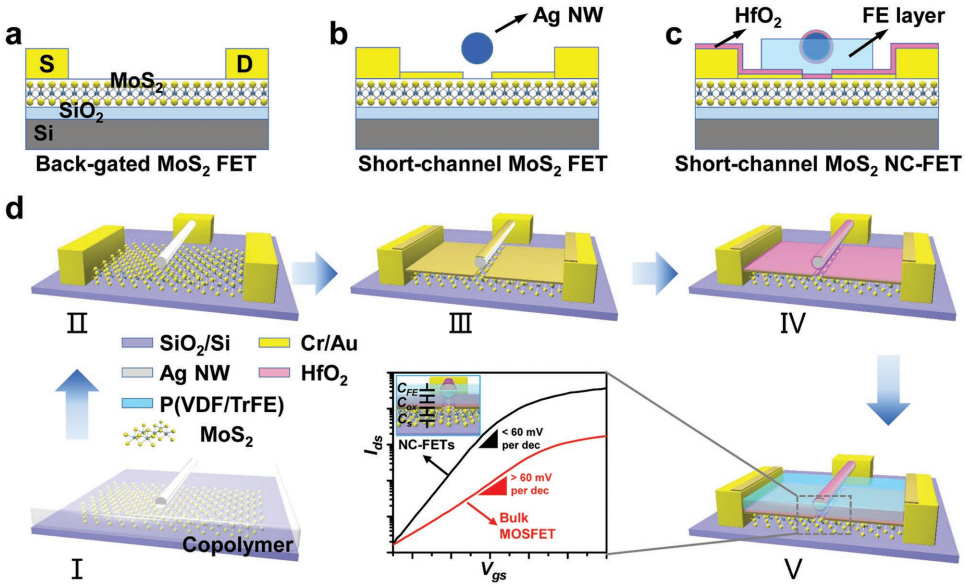

Figure 1. Schematic illustrations of MoS_2 NC-FETs. a) The cross-sectional schematic image of a traditional back-gated MoS_2 transistor with 300 nm SiO_2 as the gate dielectric. b) Top-gated MoS_2 transistors with ultrashort channel length can be obtained with a self-aligned method. c) The cross-sectional schematic image of MoS_2 NC-FETs with the implementation of ferroelectric layer. d) The fabrication process flow of self-aligned top-gated MoS_2 NC-FETs with ultrashort channel length. Copolymer layer is spin-coated onto few-layer MoS_2 followed by transferring Ag NWs; Subsequently, a PMMA (495 k) e-beam lithography photoresist is spin-coated at 4000 rpm and then baked on a hot plate at 150 °C. Standard e-beam lithography is applied to define the source, drain, and gate electrodes, followed by self-aligned metal deposition. Finally, a HfO_2 buffer layer is deposited by ALD, and ferroelectric P(VDF-TrFE) is assembled by immersing the substrate into a solution and spin-coated at 1000 rpm, and then is baked on the hot plate at 130 °C for 30 min.

is much larger than the characteristic length of the MoS_2 FET. Figure 2c is the corresponding output curves, showing linear behavior at low bias. After the self-aligned Au deposition (8 nm), a device with short L_{ch} of 85 nm is obtained, as shown in Figure 2d. The short channel MoS_2 FET displays degraded subthreshold performance, as shown in Figure 2e. Notably, the V_{th} is much larger than that of the long channel devices and severe drain-induced barrier lowering (DIBL) effect occurs.

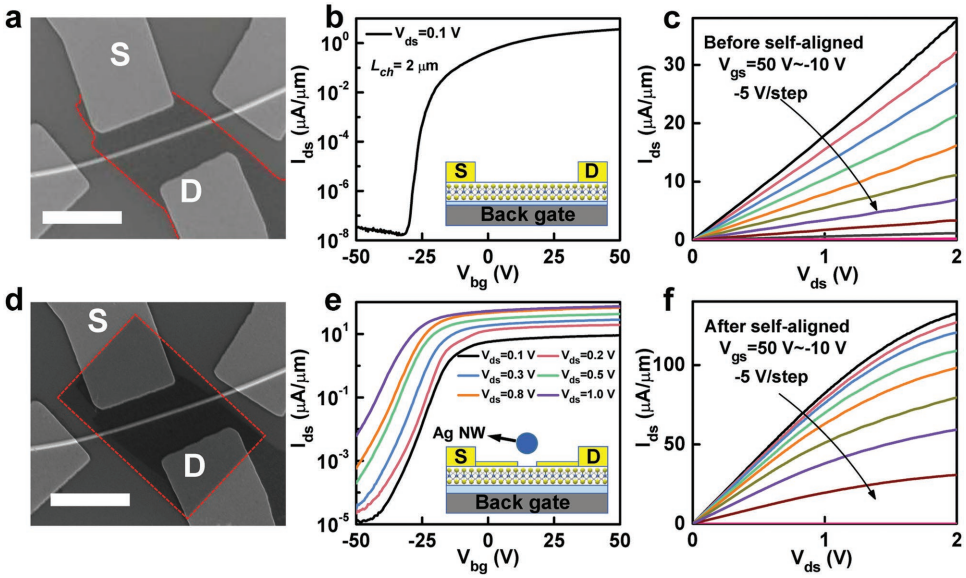

Figure 2. Electrical performance of the back-gated MoS_2 FETs at room temperature. a) The SEM image of the device, and the scale bar is 2 μm. b) Typical transfer characteristics of the back-gated few-layer MoS_2 transistors with L_{ch} = 2 μm measured at room temperature; The inset is the cross-sectional image of the device without self-aligned fabrication. c) The corresponding output characteristics of the fabricated device. d) The SEM image of the self-aligned back-gated MoS_2 transistor with L_{ch} = 85 nm; The scale bar is 2 μm. e) The transfer curves of the self-aligned back-gated MoS_2 transistors at different V_{ds} values, and the inset is the cross-sectional image of the device. f) The corresponding output characteristics of the device.

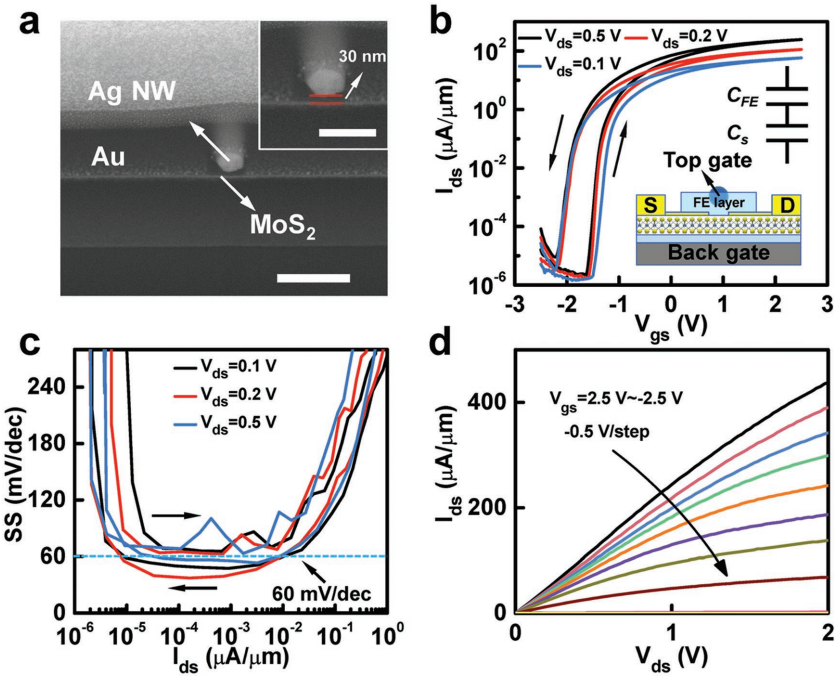

Figure 3. Electrical performance of the self-aligned top-gated MoS_2 NC-FETs at room temperature. a) Cross-sectional SEM view of the MoS_2 NC-FETs with suspended Ag NW as gate electrode and P(VDF-TrFE) as the gate dielectric layer. The scale bars in the image and inset are 200 and 100 nm, respectively. b) The transfer characteristics of the MoS_2 NC-FETs with 30 nm thick P(VDF-TrFE) as the gate dielectric layer. c) SS values as a function of the channel current at different V_{ds} values, showing minimum SS below 60 mV dec^{-1} for both forward and reverse sweeps. d) The output characteristics of the top-gated MoS_2 NC-FETs with P(VDF-TrFE) as the gate dielectric layer.

The off-state current (I_{off}) increases with V_{ds}, and the SS values increase to 4×10^3 mV dec^{-1} at $V_{ds} = 1$ V. The threshold voltage shift (ΔV_{th}) divided by the drain voltage variation is ≈27.9 V V^{-1}, indicating that the SCEs significantly affect the performance of back-gated MoS_2 transistors. As shown in Figure 2f, current crowding of the output curves is observed, and compared to the long channel devices, the current densities do not increase with the same rate of channel length shrinking. The extracted mobilities of the back-gated transistors with L_{ch} = 2 μm and 85 nm MoS_2 are 109.0 and 24.7 cm^2 V^{-1} s^{-1}, respectively. These results suggest that SCEs start to dictate the device performance.[30]

To alleviate the SCEs, short-channel top-gated MoS_2 transistors with P(VDF-TrFE) as the gate dielectric layer have been prepared, a typical cross-sectional SEM image of such devices is shown in **Figure 3**a, indicating the self-aligned Au thin film separates the MoS_2 channel through the suspended Ag NWs. The L_{ch} is slightly shorter than the diameter of the Ag NW, which means that the self-aligned process can be efficiently employed for fabricating transistors with L_{ch} in the deep nanoscale regime less than 100 nm. A suspended distance of 30 nm is observed between the Ag NW and the bottom MoS_2 layer, as shown in the inset in Figure 3a. Figure 3b illustrates typical transfer curves of L_{ch} = 80 nm MoS_2 NC-FETs with an inset schematic illustration in Figure 3b, exhibiting the on/off ratio is larger than 10^8 at room temperature. The extracted DIBL value is less than 0.5 V V^{-1}, which is much smaller than that of the back-gated transistors with 300 nm thick SiO_2 as the dielectric layer, indicating the introduction of the NC ferroelectric layer can effectively immunity the SCEs. Moreover, the smallest SS value is 37.2 mV dec^{-1} with V_{ds} = 0.1 V at room temperature, as shown in Figure 3c, suggesting that ferroelectric P(VDF-TrFE), which has obvious differential negative capacitance, could drive the electrical performance of the MoS_2 transistors to the theoretical limitations. The current range with SS < 60 mV dec^{-1} spans ≈5 orders of magnitude, and no evident gate-induced leakage is observed, as shown in Figure S3 in the Supporting Information. Figure 3d exhibits typical output characteristics of the MoS_2 NC-FETs, and the linear behavior at low drain voltage indicates that good ohmic contacts are formed at the self-aligned contact region with MoS_2.

Although NC-FET devices with SS below 60 mV dec^{-1} have been demonstrated, interfacial effects will inevitably affect the ferroelectricity of the P(VDF-TrFE) layer and further impact carrier transport in the channel. The asymmetrical charge screening effect at the top and bottom interface of the P(VDF-TrFE) layer will degrade the reliability and stability of MoS_2 NC-FETs, as demonstrated in most nonvolatile ferroelectric memory devices.[31–33] The MoS_2 NC-FETs behave with a hysteresis window (ΔV_H), which is mainly due to the capacitance mismatch and damping (resistive) term during the polarization reversion. To fit within the supply-voltage window, hysteresis window should be reduced as small as possible especially for logic switch applications.[34] Moreover, to optimize the voltage amplification effect of ferroelectric P(VDF-TrFE), an insulated dielectric layer with a matched capacitance (C_{ox}) is commonly inserted between the semiconductor and the ferroelectric layer to form a NC gate stack structure, thus making the entire system become energetically stable, including the gate stack/channel layer.[20]

In this work, HfO_2 layers are inserted as the passivation layers with a sandwich structure via ALD approach (details in the Experimental Section), as shown in the inset of **Figure 4**a. The inserted oxide layer circumvents interdiffusion problems across the interfaces and inhibit chemical reactions, so that the intrinsic properties of the ferroelectric layer and semiconductor can be conserved. For sub 0.6 V device operation, V_{ds} = 0.5 V is set for all the tests in Figure 4a (NC-FETs with $L_{ch} = 80 \pm 10$ nm is intentionally assigned), and the transfer curves of the devices are demonstrated obvious n-type on/off characteristics. Transfer curves with different gate voltage sweep rates are shown in Figure S4 in the Supporting Information to illustrate the device performance is insensitive to the sweep rate in this speed range. The comparison of the experimental data to the numerical simulation results shown in Figure 4b reveals that the subthreshold characteristics are perfectly matched with negligible gate leakage current. The numerical simulation

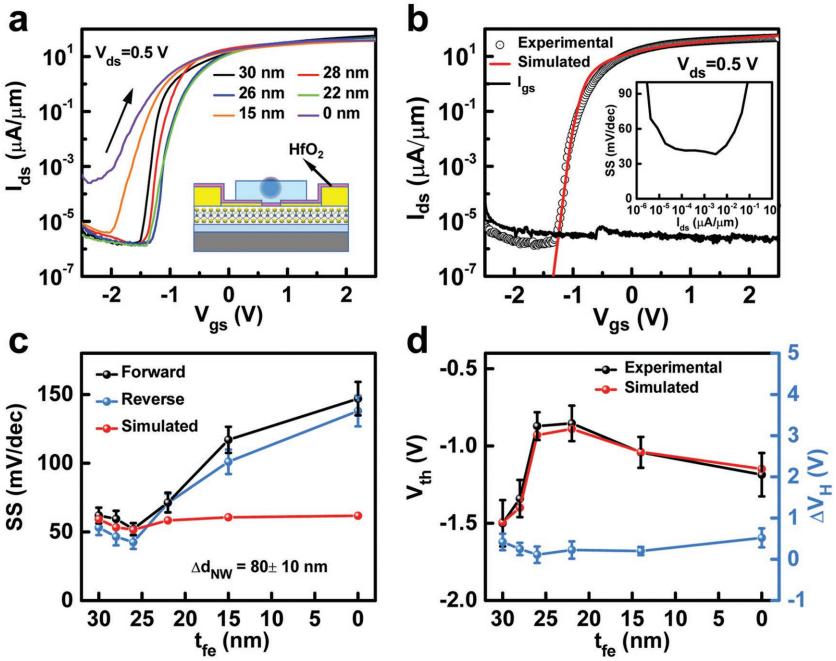

Figure 4. Electrical performance of the self-aligned top-gated HfO_2 stabled MoS_2 NC-FETs at room temperature. a) Transfer characteristics of the short channel (L_{ch} = 80 ± 10 nm) MoS_2 NC-FETs with different P(VDF-TrFE) thicknesses. b) Comparison of the transfer characteristics of the MoS_2 NC-FETs with a 26 nm P(VDF-TrFE) layer, including experimental and simulation results; the inset is the SS values as a function of channel current. c) Plots of SS versus P(VDF-TrFE) thickness. d) The V_{th} and ΔV_H of the MoS_2 NC-FETs with different P(VDF-TrFE) layer thicknesses. The error bars in (c) and (d) indicate the standard deviation over 15 devices.

results are obtained from our developed analytical model for a MoS_2 NC-FET. A negative-capacitance MoS_2 transistor with the Ag NW/P(VDF-TrFE)/HfO_2 gate stack can be approximately treated as a baseline MoS_2 transistor in series with a P(VDF-TrFE) ferroelectric capacitor.[35] In addition, the electrical behavior of a P(VDF-TrFE) ferroelectric capacitor can be described by Landau–Khalatnikov equation. Landau coefficients are extracted from the experimental P–E curve of P(VDF-TrFE) capacitors. For the baseline MoS_2 transistor, its transfer characteristics and output characteristics can be obtained by solving the Poisson equation, Boltzmann statistics law and the classical drift-diffusion transport equation self-consistently. The details about the numerical simulation are available in the Supporting Information. The inconsistent performance in the high current region is mainly due to the undesirable carrier recombination at the interfaces and inside the ferroelectric domains in the P(VDF-TrFE) layer.[36] As shown in the inset in Figure 4b, the channel current range with SS < 60 mV dec^{-1} spans ≈4 orders of magnitude. The detailed plots of SS versus P(VDF-TrFE) thickness, t_{fe}, are shown in Figure 4c, and both the SS values of the forward (from –2.5 to 2.5 V) and reversed sweep (from 2.5 to –2.5 V) directions all present the same trends and a smallest SS value of 42.5 mV dec^{-1} is achieved. This phenomenon can be explained as follows: the ferroelectric behavior is nonlinear, and the disproportionate changes in spontaneous polarization can be induced by a small supplied voltage increment, which leads to a "voltage amplification" that improves the subthreshold characteristics. Therefore, the charges momentarily exceed that of the power supply and enable the surface potential to be higher than the gate voltage, resulting in enhanced gate coupling, and thus rendering the power dissipation of these devices much smaller than that of the positive one.[8,9,30] The SS values of all the MoS_2 NC-FETs maintain an ultralow level, with a t_{fe} of ≈20 nm, and the smallest SS value can be achieved with 4 nm HfO_2 oxide layer. Due to the insertion of hafnium oxide layer, the effective thickness of the ferroelectric layer is reduced, and some of the external voltage drop across the HfO_2 dielectric layer, degrading the amplification gain of the P(VDF-TrFE) layer; therefore, the SS values intend to increase as the HfO_2 thickness approaches the spatial gap between MoS_2 and the Ag NW gate, and such a trend is also observed with the numerically simulated SS values. Conversely, this trend also indicates that the P(VDF-TrFE) ferroelectric layer, instead of the conventional high-κ dielectric (HfO_2), which is insufficient to control the channel and the contact extension regions approaching each other, can efficiently improve the electrical performance of ultrashort channel MoS_2 transistors. Although sub 60 mV dec^{-1} can be experimentally achieved, various interfacial effects will inevitably impact the ferroelectricity and further deteriorate the performance of MoS_2 NC-FETs. Therefore, all of these results in increased SS values and the mismatch of SS values between experimental data and simulated results when P(VDF-TrFE) is thinner than 20 nm, as shown in Figure 4c. Additionally, nonhysteresis operation is essential for integrated circuits, as shown in Figure 4d. ΔV_H is minimized at a low level, which is due to the improved interface properties and the HfO_2 screening some of the polarization charges. In the aggressive pursuit of device miniaturization, demonstrating the performance limit obtainable in MoS_2 NC-FETs is of significant technological relevance. The V_{th} values of the devices from both the experimental data and numerical simulation present the same trend with t_{ox}.

The transfer characteristics of more than 20 devices with L_{ch} values ranging from 42 to 130 nm are measured. As shown in **Figure 5**a, MoS_2 NC-FETs with HfO_2 (4 nm)/P(VDF-TrFE) (26 nm) dielectric stack layers exhibit evident n-type on/off characteristics. Notably, even the device with L_{ch} = 50 nm has a large on/off ratio of 3×10^5 and a small SS of 107.5 mV dec^{-1} (Figure 5a). The L_{ch} dependence of the g_m and SS values of the MoS_2 NC-FETs are plotted in Figure 5b. The SS and g_m values maintain a nearly constant level when the L_{ch} is greater than 60 nm, and as the L_{ch} further shrinks, the g_m drastically decreases with degraded subthreshold characteristics, which is originated from the SCEs. In addition, the peak g_m of 48.0 μS μm^{-1} obtained at V_{ds} = 0.5 V is comparable with the best reported values that measured at a high V_{ds} = 5 V.[37] Table S1 in the Supporting Information shows the performance comparisons among the MoS_2 transistors with similar L_{ch} to state the

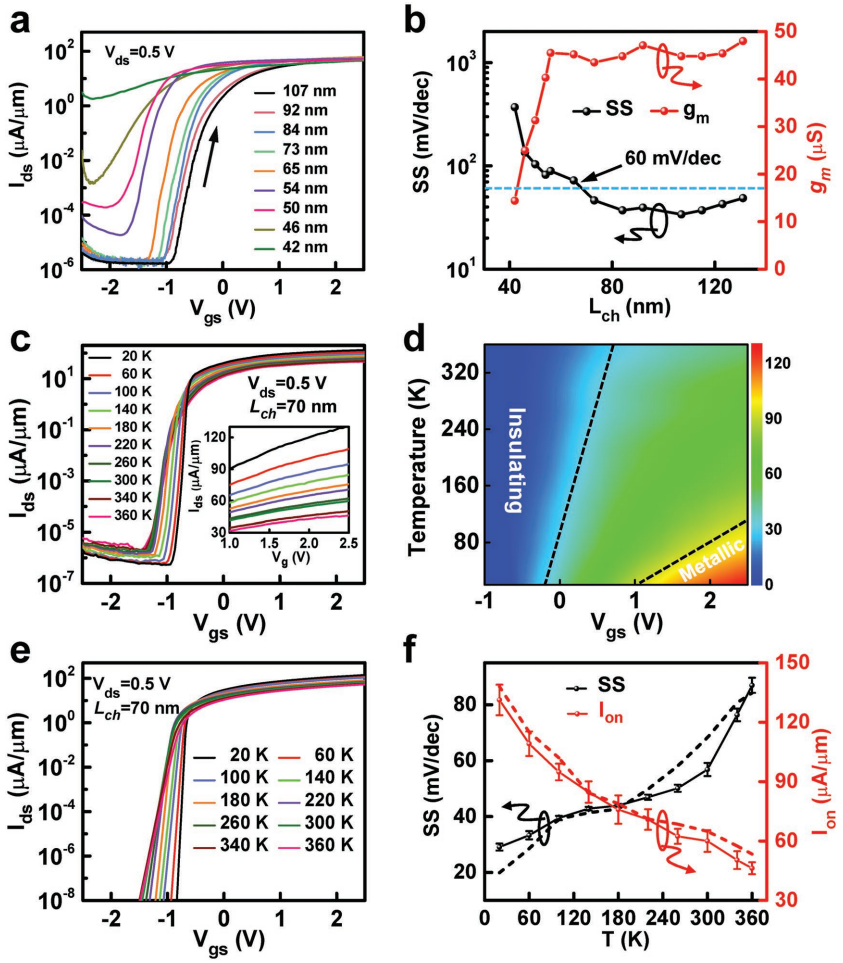

Figure 5. Scalability and low-temperature characteristics of the self-aligned top-gated MoS_2 NC-FETs. a) The transfer characteristics of the MoS_2 NC-FETs with L_{ch} values ranging from 42 to 130 nm at room temperature. b) Detailed plots of SS and g_m as a function of L_{ch}. c) Typical transfer characteristics of the MoS_2 NC-FETs measured at various temperatures, and the inset shows the detailed plots of I_{on} at different temperatures. The maximum temperature of the probe station is 360 K. d) 2D plot of current density (in unit of μA/μm) versus temperature (Y axis) and gate voltage (X axis). The guided line (black dash) illustrates the transition from insulating state to metallic state. V_{ds} voltage is 0.5 V. e) The simulation data calculated from the developed analytical model. f) SS values plot extracted from experimental data and simulated results to show the dependence with temperature. Temperature dependence of SS from 20 K layer to 360 K, and the negligible mismatch between experimental data and simulated results may come from the impact of Schottky barrier on SS. The I_{on} plots extracted from experimental data and simulated results, respectively. The error bars are the statistical analyses for 10 MoS_2 NC-FETs with the same device geometry.

significance of this work. And the current density of the MoS_2 NC-FETs is also comparable with that of the ITRS 2017 target for semiconductor on insulator (SOI) transistors, while the MoS_2 NC-FETs preserve low operation voltage and low off-state current. These results indicate that the MoS_2 NC-FETs are one of the promising successors for silicon based transistors, enabling low voltage and low-power applications.[26,27,37–43]

The MoS_2 NC-FETs exhibit distinctly different temperature dependent performance from the traditional MOSFETs, which is originated from the NC effect of ferroelectric layer, as shown in Figure 5c. The off-state current decreases as the temperature is decreased, while the I_{on} is remarkably increased (inset in Figure 5c), which gives rise to the simultaneously obtained ultrashort L_{ch} and negative-capacitance effect. The metal-insulator transition is observed, and an insulating behavior that persists until $V_{gs} = -0.13$ V. And with $V_{gs} > 1.25$ V, the devices preserve larger I_{on} at low temperature, which is the sign of metallic behavior, indicating apparently different regimes in Figure 5d. Figure 5e is the simulated results of the same devices at various temperatures, which indicates matched trends to the experimental data. In general, the electron mobility increases when the temperature decreases due to the lattice scattering is significantly reduced. And the Landau coefficients become more negative when temperature decreases. Therefore, the voltage amplification becomes more remarkable, leading to improved on-state current. The SS presents superior values less than 60 mV dec^{-1} with temperature below 300 K, and the devices still obtained a SS value of 80.5 mV dec^{-1} at a temperature as high as 360 K (Figure 5f). At low temperature below the Curie temperature (T_c), the polarization of the P(VDF-TrFE) layer leads to greatly amplified gate voltage. Although the carrier concentration is lower at low temperature, the amplification effect leads to enhanced on-state current. As the temperature is to approach the T_C, the sign of Landau parameter shifts toward positive axis. Thus, enhanced amplification effect is observed at low temperature. Therefore, the temperature-dependent property of the ferroelectric P(VDF-TrFE) layer affords the improved subthreshold characteristics at low temperature. The extracted experimental and simulated I_{on} decreases with the temperature increasing, as shown in Figure 5f. All of these demonstrate the introduction of NC ferroelectric layer in the gate dielectric stack can efficiently lower the transistors' power consumption by improving subthreshold characteristics.

Bias stress characteristics are one of the key reliability issues in field-effect transistors, which always associate with the interface traps. To investigate the electrical-stress-induced stability of the MoS_2 NC-FETs, we measured the transfer characteristics under different gate positive bias stress (PBS) and negative bias stress (NBS) conditions.[44] **Figure 6**a shows a typical evaluation of the transfer characteristics of the MoS_2 NC-FETs under PBS in the ambient atmosphere at a fixed $V_{gs} = 1.5$ V with different stress times. The I_{on} decreases and the V_{th} shifts in the positive gate voltage direction as the bias stress time increased. By contrast, under NBS conditions ($V_{gs} = -1.5$ V), as shown in Figure 6b, the I_{on} increases with the stress time, and the V_{th} shifts in the negative gate voltage direction. Notably, among both PBS and NBS investigations, the device maintains steep switching

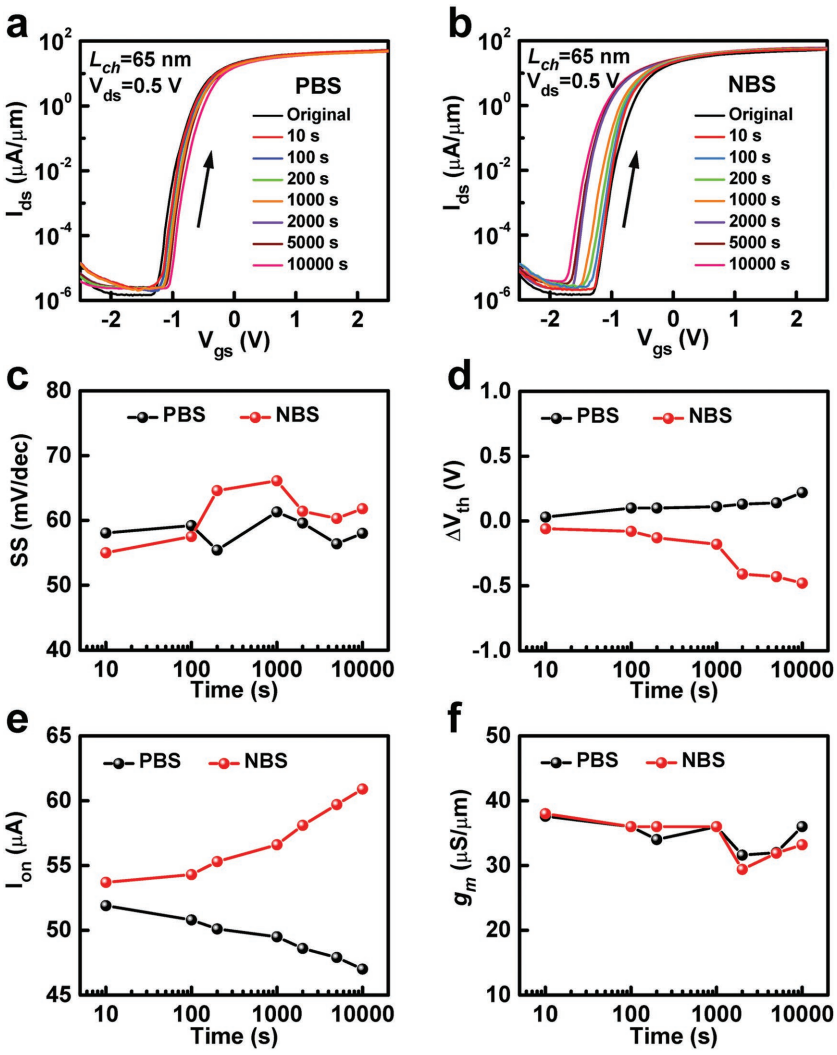

Figure 6. Electrical stability of the short channel self-aligned top-gated MoS_2 NC-FETs. a,b), The effects of PBS and NBS on the transfer characteristics of the MoS_2 NC-FETs, the channel length is about 65 nm. c–f) The detailed plots of SS and ΔV_{th}, I_{on}, and g_m versus stress time for the PBS and NBS measurements, respectively. These results indicate good reliability and stability of the developed MoS_2 NC-FETs under bias stress.

characteristics with SS values around 60 mV dec^{-1}, as shown in Figure 6c, because the HfO_2 layer prevents the interdiffusion actions at the ferroelectric P(VDF-TrFE) interfaces. The effects of PBS and NBS on the variation of V_{th} (ΔV_{th}) of the MoS_2 NC-FETs are extracted and plotted in Figure 6d. The maximum absolute values of ΔV_{th} under PBS and NBS maintain less than 0.5 V, indicating a good electrical stability of MoS_2 NC-FETs. Additionally, like silicon transistors, the ΔV_{th} is caused by the charge trapping effect at the interface between MoS_2 and the HfO_2 under electrical stress, and these also lead to the on-state current variations under bias stress, as shown in Figure 6e. Specifically, all the measurements indicate almost consistent g_m, even after 10^4 s bias stress (Figure 6f), and the slight decrements may originate from the fatigue of ferroelectric layer. All of these indicate the robust reliability and stability of the MoS_2 NC-FETs are obtained.

In this paper, we mainly focus on lowering the SS value of MoS_2 transistors to break the theoretical limit of "Boltzmann Tyranny" in traditional MOSFETs, by introducing a ferroelectric P(VDF-TrFE) layer into the top-gated dielectric stacks, forming an NC-FET. Owing to the voltage amplification effect of the ferroelectric P(VDF-TrFE) layer, steep switching performance is demonstrated with SS values as small as 42.5 mV dec^{-1} at V_{ds} of 0.5 V. Moreover, the NC-FETs exhibit significantly enhanced electrostatics control in terms of DIBL, and can suppress the SCEs as well. Furthermore, the inserted HfO_2 layer results in a stable NC gate dielectric stack layer while improving the electrical stability of the devices. The electrical performance at low temperature is also investigated from 360 K down to 20 K, exhibiting distinct behavior from the traditional MOSFETs not only with higher on-state current at low temperature, but also with nonlinear dependence of SS values as a function of temperature. Thus, 2D channel materials NC-FETs are much better than the traditional transistors in terms of the power delay product per device width, and it goes beyond overcoming the Boltzmann limit and provides the model for low-power transistors. Enabling fundamental applications through nanoelectronics research addressing SCEs and lowering the power consumption to enable fundamental applications is more rewarding now than ever.

Experimental Section

Materials Synthesis and Device Fabrication: Few layers MoS_2 flakes were exfoliated with Scotch tape on 300 nm SiO_2 coated Si substrate. Copolymer was spin-coated at a speed of 4000 rpm and then was baked on a hot plate at 150 °C. Subsequently, the Ag NWs were dispersed on the surface, and then PMMA 495k was spin-coated at 4000 rpm and baked at 150 °C. The external electrodes were defined by e-beam lithography and metallization, and an extra e-beam lithography step was conducted to enable the self-aligned metal deposition. For the top-gate dielectric fabrication, HfO_2 was deposited via ALD approach with a growth rate of 1.0 Å per cycle as follows: The tetrakis(dimethylamino)hafnium(IV) (TDMAH) precursor source was heated to 100 °C, while the H_2O source was kept at room temperature. The flow rate of Ar carrier gas was 50 sccm. The pulse times for TDMAH and H_2O are 0.1 and 0.4 s, and the postpurge times are 12 and 18 s, respectively; P(VDF-TrFE) solution was spin-coated on the substrate at 1000 rpm and annealed at 130 °C for 30 min to obtain desirable ferroelectric performance.

Materials Characterization and Electrical Measurements: SEM was conducted on Nova 450 operated at 15 kV, and the e-beam lithography was carried out on a Raith pattern generator SEM combination. Electrical measurements of the MoS_2 NC-FETs were performed on a probe station equipped with a Keithley 4200S semiconductor parameter analyzer under an ambient atmosphere and the low-temperature electrical

measurements were performed with a Lake Shore TTPX Probe Station and Agilent B1500A semiconductor parameter analyzer.

Numerical Simulation: In the modeling, the classical drift-diffusion transport mechanism of carriers is considered. The device physics mainly focuses on the impact of 2D electron gas, surface trap charges, and total source/drain series resistance on the electrical performance of the MoS_2 NC-FETs. The Poisson equation, Boltzmann equation, Landau–Khalatnikov equation, and current continuity equation are solved consistently to obtain the electrostatic potential and drain current using Newton iteration. For the low temperature simulation, the temperature-dependences of Landau coefficient and mobility are considered and model parameters are extracted from experiment measurement.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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