ACS NANO
Cite This: ACS Nano 2018, 12, 779−785
www.acsnano.org
ARTICLE

Piezotronic Transistor Based on Topological Insulators

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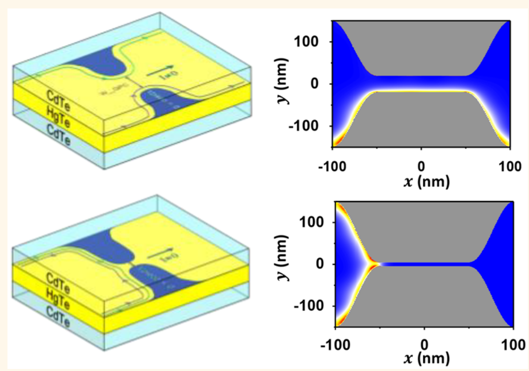
ABSTRACT: Piezotronics and piezophototronics are emerging fields by coupling piezoelectric, semiconductor, and photon excitation effects for achieving high-performance strain-gated sensors, LEDs, and solar cells. The built-in piezoelectric potential effectively controls carrier transport characteristics in piezoelectric semiconductor materials, such as ZnO, GaN, InN, CdS, and monolayer MoS_2. In this paper, a topological insulator piezotronic transistor is investigated theoretically based on a HgTe/CdTe quantum well. The conductance, ON/OFF ratio, and density of states have been studied at various strains for the topological insulator piezotronic transistor. The ON/OFF ratio of conductance can reach up to 10^{10} with applied strain. The properties of the topological insulator are modulated by piezoelectric potential, which is the result of the piezotronic effect on quantum states. The principle provides a method for developing high-performance piezotronic devices based on a topological insulator.



KEYWORDS: *piezotronics, topological insulator, quantum state, piezotronic switch, piezotronic logical unit*

Piezoelectric semiconductors have the coupling properties of a piezoelectric excitation and a semiconductor, such as ZnO, GaN, InN, and CdS. The emerging fields of piezotronics and piezophototronics have attracted much attention for flexible energy-harvesting and sensor applications.[1,2] A series of multifunctional electromechanical devices have been developed by a nanostructured piezoelectric semiconductor, such as a nanogenerator,[3−5] a piezoelectric field effect transistor,[6] a high-sensitivity strain sensor,[7] a piezophototronic photocell,[8] and an LED.[9] Piezotronic logic devices based on strain-gated transistors can convert a mechanical stimulus to a digital signal for logical computation.[10−12] Taxel-addressable matrices[13] and photon-strain sensor arrays[14] have been fabricated for integrated chips. Furthermore, nanogenerators and piezotronic transistors have been developed by single-atomic-layer MoS_2.[15,16]

For high sensitivity of piezotronic and piezophototronic devices, strain-induced piezoelectric potential plays a key role by controlling carrier generation, transport, and recombination.[17−19] The width of the piezoelectric charge distribution is an important parameter for improving performance of a piezotronic transistor. By using density functional theory, our previous theoretical studies have calculated the width of piezoelectric charge distribution in piezotronic transistors based on different metals and semiconductors.[20,21] Furthermore, piezoelectric charges change wavelength and enhance luminescence in quantum devices, such as ZnO nanowires, single-atomic-layer MoS_2, and CdTe quantum dot devices.[22−25]

Topological insulators have been revealed theoretically and experimentally based on HgTe/CdTe quantum well structures,[26−28] which have potential applications for low-energy consumption and quantum computing.[29,30] The static strain can create or destroy topological insulator states, such as HgTe and Bi_2Se_3 topological insulators.[31,32] Recent theoretical results show that the coupling of a strong electric field and strain can create topological insulator states in a GaN/InN/GaN quantum well.[33]

In this paper, a topological insulator piezotronic transistor is proposed based on a HgTe/CdTe quantum well structure. A thin HgTe layer is sandwiched between two CdTe layers to form a quantum well that has an inverted band. The strain-induced piezoelectric field modulates the electron transport in

Received: November 11, 2017
Accepted: December 24, 2017
Published: December 24, 2017

DOI: 10.1021/acsnano.7b07996
ACS Nano 2018, 12, 779−785

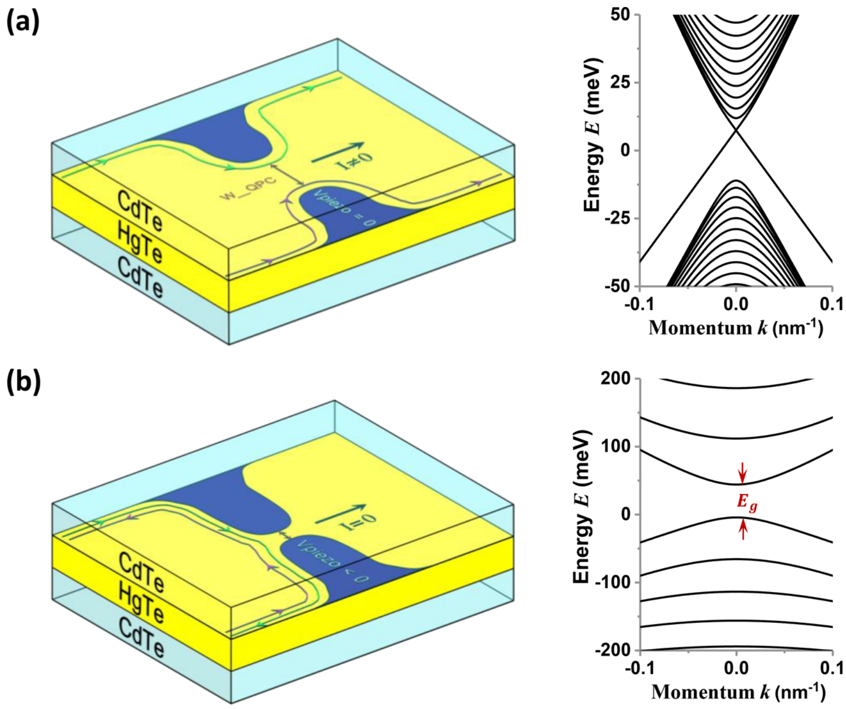


Figure 1. Schematics of electronic transport and energy band controlled by the QPC in the HgTe/CdTe topological insulator. The spin-up (green line) and spin-down (purple line) electrons travel along the boundary. (a) Gapless Dirac cone for the wide QPC and (b) energy gap E_g emerging for the narrow QPC.

the HgTe quantum wells. Therefore, the piezotronic transistor based on a topological insulator is a mechanically manipulating device using the piezotronic effect. The ON/OFF conductance ratio can reach up to 10^{10}. A piezotronic transistor based on a topological insulator can be used for a high-performance and ultra-low-power consumption switch, logical unit, and strain sensor.

To illustrate the piezotronic transistor based on a topological insulator, Figure 1 shows the HgTe/CdTe quantum well structure with a split gate on the side of HgTe. The constriction between the left and right gates acts as a quantum point contact (QPC).[34] The width of the quantum point contact can be turned by the piezoelectric potential. Figure 1(a) shows a gapless band structure in quantum point contact without a piezoelectric potential, which is a typical topological insulator based on the HgTe/CdTe quantum well structure. The current can flow across the quantum point contact region without a piezoelectric potential. This state is the "ON" state of this device. The width of the quantum point contact decreases while the piezoelectric potential increases. While the band gap is formed by applied strain, the conducting channel closes, as shown in Figure 1(b). Therefore, the electrons will be blocked and reflected back, resulting in an "OFF" state.

A piezotronic transistor based on topological insulator is a quantum piezotronic device, which uses a piezoelectric field to control the conductance of a topological insulator. The initial state is a topological insulator state without applied strain. The energy band structure of the topological insulator state changes from gapless to having a gap by applying strain. In the case of the HgTe/CdTe quantum well structure, the strain-induced piezoelectric field is parallel to the surface of the topological insulator. The direction of the piezoelectric field also can be perpendicular to the surface of the topological insulator. For example, in the case of the GaN/InN/GaN quantum well structure, the band gap becomes smaller while the strain-induced piezoelectric field increases.[33] Thus, topological insulator states are formed by a strain-induced piezoelectric field.

Besides the above two types of topological insulator based piezotronic transistor, possible structures using a piezoelectric field to control the topological insulator states are a GaAs/Ge/GaAs quantum well[35] and two-dimensional transition metal dichalcogenides,[36] such as MoS_2, $MoSe_2$, and WSe_2.

Electronic transport in the quantum well can be described by the Schrödinger equation:

$$H\psi = E\psi \tag{1}$$

where H is a Hamiltonian, ψ is a wave function, and E is an eigenvalue. By solving the Schrödinger equation under the boundary condition, the wave function can be obtained to calculate the transport properties, including the density of states (DOS), the transmission, and the conductance.

Taking a typical HgTe/CdTe quantum well topological insulator as an example, the electronic properties are described by the four-band Hamiltonian of the Bernevig−Hughes−Zhang (BHZ) model:[26]

$$H(k) = \begin{bmatrix} \varepsilon_k + M_k & Ak_- & 0 & 0 \\ Ak_+ & \varepsilon_k - M_k & 0 & 0 \\ 0 & 0 & \varepsilon_k + M_k & -Ak_+ \\ 0 & 0 & -Ak_- & \varepsilon_k - M_k \end{bmatrix} \tag{2}$$

where $k = (k_x, k_y)$ is the in-plane momentum of electrons, $\varepsilon_k = C + V(x) - Dk^2$, $M_k = M - Bk^2$, $k_\pm = k_x \pm ik_y$, $k^2 = k_x^{\,2} + k_y^{\,2}$, and $V(x)$ is the confinement potential of the quantum well. A, B, C, D, and M are the expansion parameters describing the band structure of the HgTe/CdTe quantum well. The topological

DOI: 10.1021/acsnano.7b07996
ACS Nano 2018, 12, 779−785

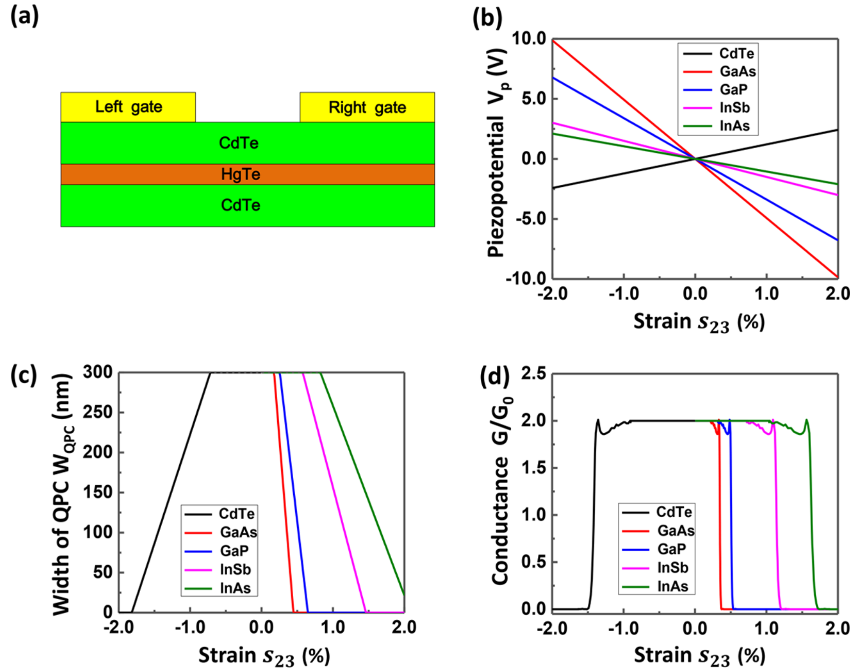


Figure 2. (a) Schematic of controlling the width of the QPC by left and right gate voltage on the top CdTe layer. (b) Piezoelectric potential as a function of strain under different piezoelectric semiconductor materials (CdTe, GaAs, GaP, InSb, and InAs). (c) Width of the QPC as a function of strain. (d) Conductance as a function of strain at fixed Fermi energy E_F = 10 meV.

property of the HgTe/CdTe quantum well depends on the thickness of the HgTe layer, which has the critical value d_c.[26] While the thickness is less than the critical thickness d_c, the quantum well is the normal insulator state. When the thickness is larger than d_c, the band energy of the quantum well is the topological insulator state. In this study, the thickness of HgTe is set at 7 nm (>d_c = 6.3 nm), a typical value for a topological insulator state of the device. The material parameters used in this study are A = 364.5 meV nm, B = −686 meV nm^2, C = 0, D = −512 meV nm^2, and M = −10 meV.[26]

The conductance is given from Landauer–Büttiker formula:[37,38]

$$G = G_0 \sum_{m,n} |t_{nm}|^2 \tag{3}$$

where t_{nm} is the transmission coefficient for an electron from the nth input mode to the mth output mode and G_0 is the conductance quantum, which is defined as e^2/h.

For a small uniform mechanical strain S, the polarization vector P is given by[39]

$$(P)_i = (e)_{ijk}(S)_{jk} \tag{4}$$

where e_{ijk} the third-order tensor is the piezoelectric tensor.

According to piezoelectric theory, the constituting equations can be given by[17,40]

$$\begin{cases} \sigma = c_E S - e^T E \\ D = eS + kE \end{cases} \tag{5}$$

where σ and c_E are the stress and elasticity tensor, E and D are the electric field and displacement, and k is the dielectric tensor.

Thus, piezoelectric potential induced by applied strain can be obtained as

$$V_{piezo} = \frac{PL_{piezo}}{\varepsilon_r \varepsilon_0} \tag{6}$$

where L_{piezo} is the length of the piezoelectric material, ε_r is the relative dielectric constant, and ε_0 is the vacuum dielectric constant.

Considering zinc-blende structure CdTe grown along the [111] direction[41] with shear strain s_{23} of the y–z plane, the piezoelectric potential is given by

$$V_{piezo} = \frac{e_{14} s_{23} L_{CdTe}}{\varepsilon_r \varepsilon_0} \tag{7}$$

where e_{14} is the piezoelectric coefficient of CdTe and L_{CdTe} is the length of CdTe in topological insulator.

For the wurtzite structure GaN[42] with strain s_{11}, s_{22}, and s_{33} along the x, y, and z directions, the piezoelectric potential can be given by

$$V_{piezo} = \frac{(e_{33}s_{33} + e_{31}s_{11} + e_{31}s_{22})L_{GaN}}{\varepsilon_r \varepsilon_0} \tag{8}$$

where L_{GaN} is the length of GaN in the topological insulator.

RESULTS AND DISCUSSION

Piezotronic Transistor Based on a Topological Insulator. Figure 2(a) shows a schematic of the strain modulation of electron transport in a quantum well. The strain-induced piezoelectric potential is applied on the left and right gate, which is located on the top of the HgTe/CdTe quantum well.[43] The split gate can affect the extension of the depletion regions of the quantum well,[44] which can restrict electrons traveling through the system. In HgTe/CdTe quantum well structure topological insulator based piezotronic devices, the split gate voltage is supplied by the piezoelectric potential and bias voltage.

DOI: 10.1021/acsnano.7b07996
ACS Nano 2018, 12, 779−785

For wurtzite structure GaN/InN/GaN quantum well, tensile, and compressive strain can induce piezoelectric charges in the interface, and a perpendicular piezoelectric field is created in the quantum well. The piezoelectric field will change the normal insulator state to a topological insulator state in the GaN/InN/GaN quantum well.

The HgTe/CdTe quantum well is a good candidate for a topological insulator for a quantum piezotronic device. The substrate of the HgTe/CdTe quantum well can be designed by zinc-blende structure piezoelectric semiconductors, such as GaAs, GaP, InSb, and InAs. According to the piezoelectric equation, the polarization charges can be obtained from eqs 4 and 5. The piezoelectric coefficient e_{14} and relative dielectric constant ε_s are listed in Table 1.[45]

Table 1. Piezoelectric Coefficient and Relative Dielectric Constant for the Crystals of Cubic Symmetry

material	piezoelectric coefficient e_{14} (C/m^2)	relative dielectric constant, ε_r	ref
CdTe	0.035	9.8	41
GaAs	−0.16	11	45
GaP	−0.1	10	45
InSb	−0.071	16	45
InAs	−0.045	14.5	45

In the case of a piezoelectric field parallel to the surface of the topological insulator, the width of the QPC can be effectively controlled by applied strain on the piezoelectric semiconductor. Previous experiments showed that the width of the QPC (W_{QPC}) is approximately linearly dependent on the split-gate voltage.[46] Therefore, W_{QPC} is proportional to piezoelectric potential in the QPC region, which is given by

$$W_{QPC} = \alpha(V_{piezo} + V_0) + W_0 \quad (9)$$

where α is the parameter depending on the topological insulator material and device structure, V_0 is the bias voltage between the left and right gate, and W_0 is the width of the QPC without piezoelectric potential. The parameters used in the calculation are $\alpha = 225$ nm V^{-1}, $V_0 = 0.87$ V, and $W_0 = 300$ nm.[46]

The piezoelectric potential is a linear function of shear strain s_{23} with different piezoeletric semiconductors, as shown in Figure 2(b). The piezoelectric potential increases with applied strain for CdTe. Due to the opposite sign of the piezoelectric coefficient, the piezoelectric potential decreases with strain for GaAs, GaP, InSb, and InAs. Figure 2(c) shows the width of the QPC at various strain from −2.0% to 2.0%.

In our simulation, the Fermi energy is $E_F = 10$ meV. At this condition, the system has one topological edge channel. Figure 2(d) shows that the conductance G changes with external strain s_{23}. The conductance changes from "ON" to "OFF" state at a strain of −1.5% in the case of CdTe. While applied strain is larger than the switching point, the band gap E_g appears. As a result, the electrons are blocked. In addition, the energy band shows a gapless structure of a topological insulator, while applied strain is less than the switching point. For GaAs, GaP, InSb, and InAs, the strain switching point is 0.36%, 0.54%, 1.21%, and 1.75%, respectively. Thus, the conductance can be effectively controlled by strain. This is the piezotronic effect on the topological insulator. The ON/OFF ratio of the conductance is up to10^{10}. Therefore, the strain-gated piezotronic transistor offers a high-performance and low-power consumption strain-gated switch, which can act as a strain-gated logic unit.

The design of a topological insulator piezotronic switch is shown in Figure 3(a). The piezoelectric potential and bias voltage are applied to the gate. The strain applied on the piezoelectric semiconductor CdTe is plotted as a function of time in Figure 3(b). The strain varies from −1.6% to −1.0%.

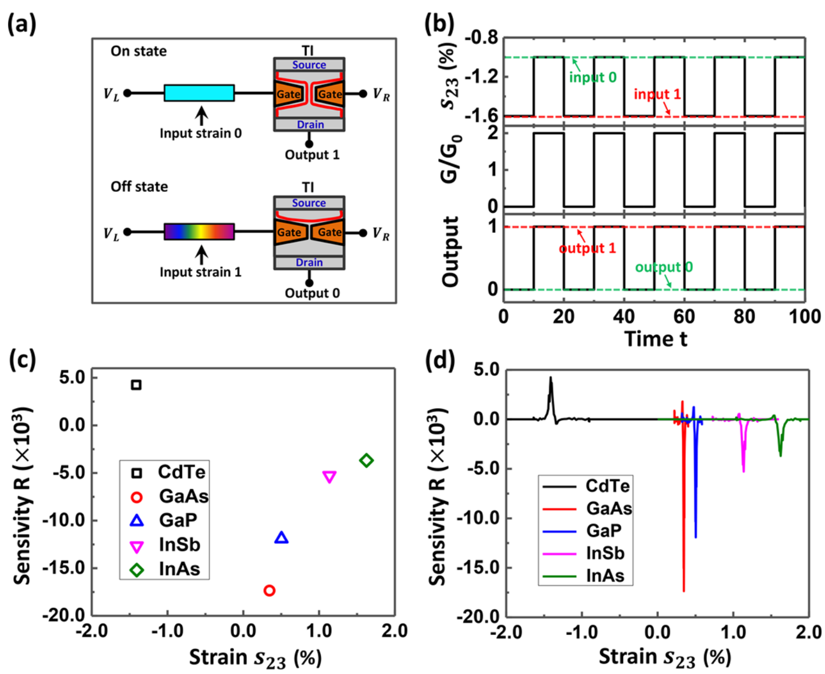


Figure 3. (a) Schematic of a piezotronic switch based on a topological insulator. The output signal 1 is the "ON" state and 0 is the "OFF" state. (b) Applied strain, conductance, and output signals change with time. (c) Maximum value of sensitivity for different piezoelectric semiconductor materials. (d) Sensitivity *versus* strain.

DOI: 10.1021/acsnano.7b07996
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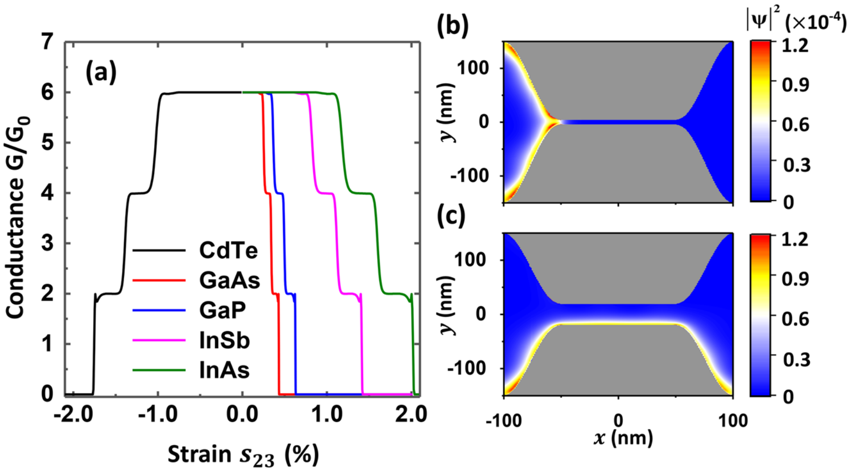

Figure 4. Conductance as a function of strain for different piezoelectric materials. The Fermi energy is fixed at $E_F = -15$ meV. Wave function of spin-down electrons (edge states): (b) OFF state at W_{QPC} = 10 nm and (c) ON state at W_{QPC} = 40 nm.

The conductance changes from near zero to $2G_0$, corresponding to the "OFF" and "ON" state, respectively.

The sensitivity of the piezotronic strain sensor can be calculated by

$$R = \frac{d(G/G_0)}{ds_{23}} \tag{10}$$

The maximum values of sensitivity and corresponding strain are shown in Figure 3(c). It clearly shows that the maximum sensitivity is larger than 10^3, For GaAs and GaP, the maximum value of sensitivity can reach over 10^4. Figure 3(d) shows the switch and strain sensor region divided by the sensitivity. The amplitude of the sensitivity sharply changes at the sensor region.

Piezotronic Effect on Surface States of a Topological Insulator. Topological insulators based on HgTe quantum well structure have gapless surface states and an insulating bulk. Figure 4(a) shows the conductance of the topological insulator surface as a function of strain. The Fermi energy is fixed at $E_F = -15$ meV. The local densities of states (LDOS) of spin-down electrons for "OFF" and "ON" states are shown in Figure 4(b) and (c), respectively. In our simulation, the calculated widths of the QPC are W_{QPC} = 40 and 10 nm, corresponding to a strain of −1.67% and −1.78%, respectively. The spin-up properties can also be obtained by the KWANT software package.[47] The surface states of topological insulators present strain-modulated transport properties by using the strain-induced piezoelectric field.

Previous theoretical results presented that the more conducting channels from bulk states can be created while the Fermi energy increases.[34,48] There are three channels: one is an edge channel and two are bulk channels, as shown in Figure 4(a). Three conductance plateaus can be created while the strain changes. Each conducting channel contributes a conductance ($2e^2/h$) to the total conductance. In the case of the HgTe/CdTe quantum well, the edge channel in the QPC is created while the strain changes from −1.74% to −1.48%. While the strain increases from −1.32% to −1.17%, the width of the QPC increases. One bulk channel in the QPC is formed, which contributes a conductance plateau to double the total conductance. This is the mechanism of the second conductance plateau. While the strain increases from −0.92% to 0, the third conductance plateau appears. The conductance steps are plotted for GaAs, GaP, InSb, and InAs, as shown in Figure 4(a).

CONCLUSIONS

In this study, we have proposed a strain modulation of electronic transport in a topological insulator. Two types of piezotronic transistors have been demonstrated based on topological insulators of HgTe/CdTe and GaN/InN/GaN structure, corresponding to a normal open and normal closed switch, respectively. The strain-induced piezoelectric potential is used to control the width of the QPC and affects electronic transport of the piezotronic transistor based on a topological insulator. A transition is shown when the conductance changes from near zero to the conductance, which presents a high ON/OFF ratio of 10^{10}. Piezotronic logical unit and high sensitivity strain sensor can be designed by the strain-gated piezotronic switch. Furthermore, the multiple conductance steps for higher Fermi energy are investigated at various strains. This study provides not only the guidance for developing high-performance piezotronic spin devices but also theoretical insight into using piezotronic effects on physical properties of spin transport.

METHODS

The conductance of this quantum spin Hall system is calculated by KWANT code. KWANT is free software and has obtained wide application in the numerical calculation of quantum transport in nanostructure systems. KWANT solves the scattering problem by using the wave function approach.

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Author Contributions

G.H. and Y.Z. contributed equally to this work. G.H., Y.Z., and Z. L.W. designed the system, and G.H. and Y.Z. performed the calculations, analyzed the data, and wrote the paper. L.L. analyzed the data. Z.L.W. supervised the study, analyzed the data, and revised the paper.

DOI: 10.1021/acsnano.7b07996
ACS Nano 2018, 12, 779−785

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors are thankful for the support from University of Electronic Science and Technology of China (ZYGX2015-KYQD063), Swansea University, the SPARC II project, the AgorIP project, the Innovate UK, and Thousand Talents Program for a Pioneer Researcher and His Innovation Team, China.

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